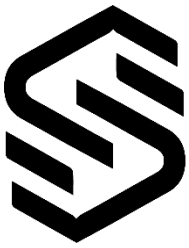

StarFive
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VIC7100

DATASHEET

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REVISION HISTORY

Version	Changes	Date
01.01.01	1. Initial release.	2021-3-5
01.01.02	1. Add Peripherals Port Memory Map Table in Section 5. 2. Add Function IO Share with Interface Group Table in Section 10. 3. Add Signal Full MUX with GPIO Table in Section 10.	2021-3-12
01.01.03	1. Added Chapter 3 which lists the IP block suppliers. 2. Added Chapter 11 which describes the various signals that get shared on the package pads FUNC_SHARE_PAD and GPIO_PAD. 3. Added Chapter 12 which lists the configuration registers associated with the GPIO pads. 4. Fixed overall formatting of the document.	2021-3-30
01.01.04	1. Updated the IP block list in Chapter 3. 2. Removed Watermark. 3. Fixed minor typos.	2021-4-19

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1. Introduction

Highlight Features:

- RISC-V U74 Dual core with 2MB L2 cache, support Linux; 1.0GHz
- Vision DSP Tensilica-VP6 for computing vision
- NVDLA Engine 1 core (configuration 2048 MACs@800MHz)
- Neural Network Engine (1024MACs@500MHz)
- 2xchannels of 32bit LPDDR4/DDR4, 3200Mbps(25.6GB/s), high efficiency required
- Video Decoder(H264/H265) up to 1 channel 4K@60fps or 8 channel 1080p30fps
- Video Encoder(H264/H265) up to 1 channel 4K@60fps or 8 channel 1080p30fps
- Dual channels of ISP, each channel support up to 4K@30fps
- Support Up to 3 video input, 1x for DVP and 2x for MIPI-CSI with 4D2C up to 4K@30fps
- Support LCD or MIPI-DSI output up to 4K@30fps
- Support MIPI-CSI TX for video output after ISP and AI processing
- JPEG Encoder/Decoder up to 8M@30fps
- USB3.0/2.0 Host/Device mode
- Support Ethernet MAC 1000Mbps
- Support TRNG and OTP
- Support DMAC, QSPI and other peripheral
- Dedicated Audio Processing DSP and sub-system

2. Feature List

2.1. CPU Subsystem

2.1.1. Overview

- 64-bit High performance RISC-V CPU (U74) Dual cores for main general computing
- 32bit RISC-V CPU core (E24) for low power and real control/configure tasks as Co-processor
- L2-cache up to 2MB cache size
- Easy Master (EZMAST) works as event co-processor for high efferent events handling
- Dual DMA controller for memory-to-memory and memory-to-peripheral data exchange
- Support Linux/VxWorks/RTOS

2.1.2. SiFive U74 Dual Core

- Fully-compliant with the RISC-V ISA specification
- Dual-core with Cache coherence
- RV64GFC U74 Application Core, each core has
  - 32KB L1 I-cache with ECC (8-way)
  - 32KB L1 D-cache with ECC (8-way)
  - 8 Region Physical Memory Protection
  - Embedded MMU support Linux OS
  - Sv39 Virtual Memory support with 38 Physical Address bits
  - PMP with 8 regions and a minimum granularity of 4096 bytes.
- CLIC for timer and software interrupts
- PLIC with support for up to 127 interrupts with 7 priority levels
- Support SCIE (SiFive Customer Inst Extension)
- Support JTAG as Debug port
- Support Multiple AXI Interface including system, peripheral, memory port and front port

2.1.3. SiFive E24 Core

- Fully-compliant with the RISC-V 32 ISA specification

- RV32IMAFC E24 Core
  - 16KB I-cache with 32 Byte cache line
  - 64KB TIM with two banks and atomic operation
  - 4 Region Physical Memory Protection
- CLIC with support for up to 127 interrupts with 16 priority levels
- Support JTAG as Debug port
- Support AHB-Lite system bus for2GB memory map

2.1.4. EZMAST

- AHB master and AHB slave port
- When CPU power down, it can operate bus through event trig
- Support 128 events
- 25 opcode

2.1.5. DMA

- Support general DMA operation and Scatter Gather DMA.
- Support up to 16+4 channels
- Support up to 32 requests, the detail configured request number is TBD
- Support AXI4 bus interface
- Support AXI Bus width of 64/128 bits
- Supports memory to memory, memory to peripheral, peripheral to memory and peripheral to peripheral transfer.
- Transfer complete interrupts and error interrupts are generated.
- Arbitration supported - fixed and round robin.
- Provides Status of each transfer through status register for each channel.
- Support 4+4 Scatter Gather channels in all 16+4 channels

2.2. Memory and Storage

2.2.1. On Chip Memory

- BUS RAM up to 256KB

- Shared BUS memory with DLA 2MB
- Boot ROM up to 32KB

2.2.2. DDR

- DDR controller
  - Support 2 channel of x32
  - DDR4/3 and LPDDR4/3 modes & signaling, rates up to following speed:
    - 2133Mbps (DDR3/LPDDR3)
    - 3200 Mbps (DDR4/LPDDR4)
  - Internal de-skew PLLs for high speed, low jitter clock generation (clk4x)
  - x16/x32 data path interface extendable
  - DRAM ranks of 1, 2 (could be asymmetric)
  - Bank-interleaving & rank-interleaving (symmetric ranks only)
  - Support for dynamic DRAM frequency scaling
  - Automated clock gating of internal logics
  - Error-correction code (SECDED) to select DRAM memory space
  - Address region based security control support
  - Automated low power control of DRAM devices
  - AMBA AXI4 protocol for main data path interface for DDR controller
  - AMBA APB4 protocol for configuration register access interface for DDR controller
  - Flexible refresh control
    - Automated adjustment of refresh interval
    - Pulled-in or postponed of refreshes
    - Dynamic per-bank / all-bank refresh switching
    - Opportunistic advanced per-bank refresh
  - Open page based advanced page policy
    - Programmable timeout pre-charge
    - Auto pre-charge for reducing command congestion
  - Independent read and write timing adjustments with auto calibration
  - Various power-down modes for low power including self-refresh support

- DFI 4.0 specification between DDR controller and DDR PHY

- DDR PHY
  - High resolution write/read timing control
  - Per-bit de-skew on the write data path
  - Per-bit de-skew on the read data path
  - Support for multiple leveling/training modes through PHY evaluation mode
  - Register programming interface to all PHY parameters
  - PHY independent mode training logic
  - Write/read data timing per-chip select
  - Low-power modes
  - Low-speed test interface (PHY BIST)
  - At-speed ATPG support (OPCG)
  - DBI support
  - PHY controller frequency ratio of 2:1
  - IO calibration
  - JTAG interface
  - Boundary scan support
  - Testability features

2.2.3. QSPI

- QSPI master controller
- Programmable master mode
- Data rate up to 100M bps per bit
- 1/2/4 data bit
- Support XIP mode and Boot mode
- Separate data input and output bit

2.3. Vision and AI Computing

2.3.1. VP6

- Highly efficient 32-bit base architecture

- Extend with designer-defined, application-specific instructions, execution units, register files, and I/Os
- 7-stage pipeline depth for core instruction set architecture (ISA)
- Histogram operations
- Up to 32 interrupts
- Local memories configurable up to 256KB ITCM and 256KB DTCM
- 32KB instruction Cache
- Up to 128b-wide flexible-length instruction extensions (FLIX) instructions
- Multi-core on-chip debug (OCD) with break-in/break-out
- Dual-load/stores each up to wide with data cache support and multi-bank RAM support
- Compatible interfaces for ARM® CoreSight™ debug and trace technology
- IEEE 754-compliant single-/double-precision scalar floating-point unit
- 1 AXI Master port and 1 AXI Slave port
- single-channel integrated DMA engine
- Complete matching software development tool chain
- Support generic RTOS Compatibility

2.3.2. DLA

- NVDLA based
- High-performance convolution core with 2048 MACs
- Supports various image input formats
- Dedicated Depth-wise Convolution engine
- Acceleration engine for Activation functions
- Acceleration engine for Pooling
- Acceleration engine for advanced Normalization functions
- Memory-to-memory transformation acceleration for tensor reshape and copy operations
- 2MB local on-chip SRAM, shared by AXI slave port accessed by other BUS master

2.3.3. NNE50

- Input feature map size (Width x Height): No Limited
- Precision: INT8

- Normal and Depth-wise Convolution Operations
- Non-normal Convolution Operations (such as transposed convolution, dilated convolution)
- Pooling Operations
  - Average Pooling, and Maximum Pooling Algorithm
  - Size (Width x Height): 2x2, 4x4
- Element-wise Operations
  - Element-wise addition, and multiplication are both support
- Activation Operations
  - ReLU, LeaklyReLU, LReLU, Tanh, Sigmoid, and other types of non-linear activation functions are all supported.
- Fully-Connected Operations
  - There is no limit on input feature map size, however, large connections might degrade NNE50 performance because of the restriction of on-chip SRAM size.
- Shortcut Operations
  - Currently only 1 frame shortcut is support.
- Batch Normalization are support.

2.3.4. VAD

- Ultra-low power Voice Activity Detector for audio bit-stream as a Voice Trigger
- Speaker/Silence detection; Data buffering wrapped for command recognition
- Configurable multi-channel (1-4) support both output of ADC(AMIC) and PDM(DMIC)
- Support 16KHz sample rate; 16-bit precision
- Up to 128K bytes ring buffer reload address can be configured by software

2.4. Video Processing Subsystem

2.4.1. Camera MIPI IN/OUT Interface

- CSI-2 RX Controller
  - Support of the MIPI CSI-2 v1.3 protocol over D-PHY PPI interface up to maximum 4*1.5Gbps.
  - Pixel interface supporting.
  - Byte to pixel conversion one-pixel interface.

- Direct memory dump using packed byte operation.
- Flow control.
- Payload FIFO operation.
- Monitoring of frame for automatic start/end of frame synchronization when enable.
- Extended Functions for Virtual Channel extension and RAW16/20 modes as defined for MIPI CSI-2 V2.0 Specification.
- Enable by setting v2p0_support_enable bit in the static_cfg configuration register.
- RAW16/RAW20 become valid data types.
- VCX (Virtual Channel Extension) will be employed - Effects ECC handing.

- MIPI RX D-PHY
  - Supports standard 8b PPI interface compliant of MIPI D-PHY spec
  - Supports total up to 6 lanes in D-PHY and data rate up to 1.5Gbps
  - Support 1 clock Lane and up to 4 Data Lane scalability in DPHY mode
  - Supports independent (1 Clock Lane and up to 2 Data lanes) x2 in DPHY mode
  - Supports lane swap in MIPI D-PHY configuration for convenient package and PCB board routing.
  - Supports clock and data lane swapping function
  - Support Triggers, ULPS and LPDT.
- CSI-2 TX Controller
  - CSI-2 Protocol handling
  - CSI-2 interface up to a maximum of four 2.5Gbps data lanes
  - High Speed data transmission
  - Automatic LP control for clock and data lane power saving
  - Automatic synchronization short packets generation (frame start, frame end, line start, line end)
  - Automatic frame counting when enabled
  - Automatic line counting when enabled
  - Pixel byte-to-packet conversion
  - Virtual Channel/Data type interleaving
  - Protocol error detection
  - Interrupt generation
  - Bypass mode

- Share MIPI TX DPHY with DSI controller

2.4.2. ISP

- Sensor Interface
  - Support up to 4K (3840x2160) pixels @30fps CMOS RGGB image sensor
  - Support one MIPI and one DVP sensor input interface
  - Support 12-bit sensor data input
- Image processing engine
  - Built-in color pattern generation
  - Sensor black level compensation
  - Defective pixel correction
  - R/G/B LUT for sensor linearization correction
  - Image analysis for AE, AWB and AF
  - Programmable histogram analysis
  - White balance control
  - Lens shading compensation
  - Color shading compensation
  - CMOS sensor spatial crosstalk cancellation (Gr and Gb balance filter)
  - Advanced Bayer CFA color interpolation
  - False color suppression
  - Advanced edge control and enhancement
  - R/G/B Gamma LUT
  - Color correction matrix
  - Color space conversion
  - Brightness/contrast and hue/saturation adjustment
  - Global tone mapping
  - Spatial noise reduction
- Back end processing
  - Seamless digital scale down from 1/4x to 1x
  - Support up to 3 channel video streaming

2.4.3. Video Encoder

- 4K 60frames X1 channel/sec or 1080p 30frames X8 channel/sec @ 500Mhz
- H.265/HEVC Encoder
  - Fully compatible with ISO/IEC 23008-2 High Efficiency Video Coding Main/Main10/MSP(Main Still Picture) Profile
  - I/P slices
  - CTU64
    - Supported Prediction Unit(PU) size: 32x32, 16x16, 8x8
    - Supported Transform Unit(TU) size: 32x32 to 4x4
  - Parallel tools
    - Wavefront parallel processing (WPP) encoding with a single slice
    - Multi slice: Independent slice segment and dependent slice segment
  - High performance offline CABAC encoding
  - Motion estimation
    - 1/4-pel precision motion vectors
    - Search range [+/-128H, +/-64V] with an adaptive search center
    - Two reference frames for P-slice
    - Long-term reference for P picture and B picture
    - Custom tuning tools
    - Custom Lambda map and lambda table
    - Custom mode decision
    - Fully programmable user scaling list
  - In-loop Filter
    - De-blocking filter
    - Sample adaptive offset (SAO)
    - Loop filtering across slices
  - Weighted prediction
  - Strong intra smoothing on/off
  - Transform skip
  - Lossless coding

- Picture/CTU/sub-CTU level of rate control
- Region of Interest (ROI) encoding with custom QP map
- Background encoding
- 3DNR

- H.264/AVC Encoder
  - Compatible with the ITU-T Recommendation H.264 specification. All coding tools in the profiles are supported.
  - With a few exceptions:
    - Interlaced coding tools are not supported.
    - FMO/ASO tool of H.264 is not supported.
  - 16x16, 8x8 and 4x4 block sizes are supported and configurable.
  - Motion estimation
    - 1/4-pel accuracy motion estimation with programmable search range up to [+/-64H, +/-32V]
    - B picture with bi-prediction
    - Two reference frames for P-slice
    - Long-term reference for P picture and B picture
    - Intra prediction
    - Luma I4x4 Mode : 9 modes
    - Luma I8x8 Mode : 9 modes
    - Luma I16x16 Mode : 4 modes (Vertical, Horizon, DC, Plane)
    - Chroma Mode : 3 modes (Vertical, Horizon, DC)
  - Custom tuning tools
    - User-defined mode(skip,intra) map
    - User-defined QP map
    - Lambda tuning for custom mode decision
    - Fully programmable user scaling list
  - Weighted prediction (optional)
  - In-loop de-blocking filter
  - CABAC/CAVLC support
  - Error resilience tools:

- CIR (Cyclic Intra Refresh)
- multi-slice structure

- A frame level and MB level of rate control
- Region of Interest (ROI) encoding with custom QP map

2.4.4. Video Decoder

- 4K 60frames X1 channel/sec or 1080p 30frames X8 channel/sec @ 450Mhz
- Support Format 420, 8-/10-bit
- Support I/P type slice
- HEVC Main/Main10, L5.1
- H.264 High/High10, L5.2
- 128bit AXI Bus interface
- Support Lossless Compression for frame buffer to save bandwidth
- Frame-based Processing promising the lowest burden to host processor for video operation
- Generating an interrupt when(ever) a specified number of MB-/CTU-rows are reached for low delay decoding
- H.264 decoding tools including:
  - Compatible with the ITU-T Recommendation H.264 specification
  - Supports MVC Stereo High Profile
  - Supports CABAC
  - Supports CAVLC
  - Variable block size (16x16, 16x8, 8x16, 8x8, 4x8, and 4x4)
  - *Interlaced coding tools are NOT supported
  - *FMO/ASO is NOT supported
- HEVC decoding tools including:
  - Compatible with ISO/IEC 23008-2 High Efficiency Video Coding
  - I/P slices
    - All intra-prediction modes
    - All inter-prediction modes
  - Variable CTU size : 64x64 to 16x16
    - Variable Prediction Unit (PU) size : 64x64 to 4x4

- ◆ Variable Transform Unit (TU) size : 32x32 to 4x4
- − Advanced Motion Vector Prediction (AMVP) and merge mode
- − ¼ Motion compensation with 8 tap filters
- − Uniform reconstruction quantization (URQ)
- − High performance CABAC decoding
- − In-loop de-blocking filtering
- − Sample Adaptive Offset (SAO)
- − Loop filtering across slice/tile boundaries
- − Data reporting to the external host
- − Robust error concealment
- − Sequence change detection

2.4.5. JPEG

- 290MPixel/sec for YUV420, 210MPixel/sec for YUV422, 140MPixel/sec for YUV444 @200Mhz
- Bit rate 480Mbps (MJPG 8M 30fps 422 1:8)
- Baseline/Extended sequential ISO/IEC 10918-1 JPEG compliance
- Compliant with Motion JPEG
- Support 1 or 3 color components
- 8-bit or 12-bit samples for each component - configurable
- Support 4:2:0, 4:2:2, 4:4:0, 4:4:4 and 4:0:0 color format (max. six 8x8 blocks in one MCU)
- Support from 16x16 pixels to 32K x 32K (32,768x32,768)
- Support ROI (Region of Interest) - decoder only
- Support 422/444 packed mode for all color formats
- After conversion to 422/444 color format
- Value-added Features for Encoding
  - − Partial mode for encoding
  - − On-the-fly rotator / mirror
- Value-added Features for Decoding
  - − Partial mode for decoding
  - − ROI (Region of Interest)

- On-the-fly rotator / mirror
- On-the-fly down sample

2.5. Display Subsystem

2.5.1. Display

- RGB656, RGB888 I/F, up to 1080p@60fps display
- Support 1/64-64 times scaler (1/64 not covered)
- Support MIPI TX DPHY lane connected with panel module

2.5.2. MIPI Display Interface

- MIPI TX DPHY
  - Supports standard 8-bit/16-bit PPI interface compliant to MIPI D-PHY spec.
  - Supports 1 Clock Lane & up to 4 Data Lanes scalability.
  - Supports MIPI D-PHY HS-Tx data rate from 80Mbps up to 2.5Gbps. (< 0.1ppm/step)
  - Supports MIPI D-PHY LP-Tx data rate of 10Mbps.
  - Supports Triggers, ULPS and LPDT.
  - Supports MIPI DSI and MIPI CSI applications.
  - Integrates switchable on-die termination.
  - Supports clock and data lane swapping function.
  - Supports reverse direction ULPS and LPDT.

2.6. Connectivity Subsystem

2.6.1. USB 2.0/3.0

- USB2.0/3.0 controller
  - USB Interface:
    - Compliant with USB 3.0 Specification
    - Compliant with xHCI 1.0 Specification
    - SuperSpeed, Hi Speed and Full Speed supported
    - Single USB2.0 Port

- Single USB3.0 Port
- USB 3.0 PIPE interface compliant
- USB 2.0 UTMI+ interface compliant
- USB2 L1/L2 Support
- USB3 U1/U2/U3 Support

- Application Interface:
  - AXI3/4 Master Interface with 64-bit data and 32-bit address
  - APB4 Slave interface with 32-bit data and address
- Dual Mode Operation:
  - HW selectable default mode selection supporting operation without any SW interaction
  - Programmable runtime mode change
  - Host Negotiate Protocol (HNP) support
  - SRP support
  - Separate Power Domains for Host and Peripheral Device logic
- Host Mode (CDNSXHCI):
  - Configurable total slots supported (maximum of 3264)
  - 32 endpoints per slot
  - 256 Primary Streams supported
  - MSI Support
  - Root Hub functionality implemented
  - xHCI Dynamic and Static Low Power Management Support
  - xHCI DMA engine with 64-bit @ 125MHz Full Duplex Data Path
- Peripheral Mode (USBSS-DEV):
  - Control transfers supported by Endpoint #0
  - Up to 15 IN and 15 OUT configurable/ programmable endpoints
  - Scatter-gather DMA
  - Dynamic data buffering
- Integrated Protocol Stack
  - Memory integration
  - Clock, reset and power management integration

- USB3.0 PHY
  - 5.0-Gbps super-speed data rate through 3m USB3.0 cable.
  - Supports 25MHz clock inputs.
  - Supports down-spread Spread Spectrum Clock (SSC) transmission and receiving (0~-5000ppm).
  - PIPE3.0 compliant interface for USB3.0.
  - Supports 16-bit interface at 250MHz operation and 32-bit interface at 125MHz operation.
  - Supports super-speed power down modes: U0, U1, U2 and U3.
  - Integrated PHY with TX, RX, SSC, PLL, digital core and ESD.
  - With adaptive RX equalizer to support different channel conditions.
  - Accessible programmable controls allows user specific optimization of critical parameters.
  - Integrated PLL to provide a variety of stand-alone clock outputs for USB related applications (25, 30, 48, 60, 120, 125 and 480MHz).
  - Provides robust BIST function for mass production tests.
  - Built-in SSTX de-multiplexing and SSRX multiplexing for type-C or dual connectors.
- USB2.0 PHY
  - 480-Mbps high-speed, 12-Mbps full-speed and 1.5-Mbps low-speed data transmission through 5m USB2.0 cable.
  - Supports USB2.0 normal mode, suspend, resume and remote wakeup.
  - Compliant with UTMI+ interface (High-speed, Full-speed, Low-speed and Preamble Packet).
  - Supports all USB2.0 test modes.
  - Built-in 45Ω termination and 1.5KΩ pull-up resistor.
  - SYNC and EOP generation and checking.
  - NRZI encoding and decoding.
  - Accessible register controls allow user specific optimization of critical parameters.

2.6.2. Ethernet GMAC

- Compliant with IEEE 802.3 specifications
- Support for IEEE 1588-2002 and IEEE 1588-2008 standards including:
- IEEE 802.3-az for Energy Efficient Ethernet (EEE)
  - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion.

- IEEE 802.1Q VLAN tag detection for reception frames

- Support data transfer rates of 10/100/1000 Mbps
- Multiple TCP/IP offload functions supported
- Power Management Module (PMT) with remote wake-up frame and magic packet frame processing
  options
- RGMII, GMII, RMII, MII interface to communicate with an external gigabit PHY.

2.6.3. CHIPLINK

- An off-chip serialization of the TileLink protocol, used to connect to an optional expansion board.
- It is implemented as a source-synchronous single-data rate parallel bus.
- Off-chip cache-coherent bus masters (e.g., in an FPGA)
- Off-chip memory-mapped slave devices
- Credit-based flow control to absorb off-chip latency
- Out-of-order completion to unblock concurrent operations
- Devices in the FPGA to connect their interrupts to the PLIC via this ChipLink bus.

2.6.4. SD/SDIO/eMMC Host Controller

- 2 sets of Host Controller for SDIO devices
- 4-wire mode only
- Support up to 100MHz
- Support SD device of SD/mmc/SDIO WIFI module

2.7. Audio Interface

2.7.1. I2S

- Up to 4 set of I2S I/F (one for RX and three for TX)
- All I2S module support standard I2S format
- Support programmable sample rate: 16K/44.1K/48KHz
- Data resolution support up to 24bit (programmable support 16bit)
- Programmable FIFO depth up 32 for each channel

- All I2S module FIFO support DMA interface
- On-chip ADC or DAC can be bypassed with external codec device

2.7.2. S/PDIF

- 2 sets of S/PDIF, one for RX and one for TX mode
- Support sample rates from 44.1kHz up to 192kHz.
- Support PCM format with a resolution of 16-bits or 24-bits per sample

2.7.3. PDM

- Support up to 4 channels with same sample rate
- Pulse Density Modulation interface for digital MIC interface
- Clock: 62.5K ~ 4MHz
- Down sampling to 24bit in SRC
- Combine clock source for each 2 channels
- I2S interface connect with I2S internally

2.7.4. PWMDAC

- The data format is 16bit, 8bit
- Support most sampling frequencies
- FIFO depth 8-byte
- Support two channels
- The resolution of PWM-DAC audio sampling supports 10bit and 8bit
- Data handling, software mode and DMA mode

2.8. Security Subsystem

2.8.1. Encryption Engines

- AES
- SHA
- ECC
- HASH

2.8.2. TRNG

- Compliant with NIST SP800-90a/b/c and BSI AIS 20/31
- Internal random seeding operation
- Host driven non-seeding option
- start-up continues and on-demand health test
- 128-bit random number generation
- 128 bits of security strength

2.8.3. OTP

- VDD and VDD2 Power Supply: 0.9V VDD, 1.8V VDD2 for Read and Program
- Memory Organization 512 x 32-bits (2KB).
- Bit Program Operation
- Data Retention: >10 Years
- Access Time: 50ns (max)
- Bit cell Program Time: 10us (min)

2.9. System Peripherals

2.9.1. SPI

- Up to 4 sets of SPI controller support Slave and Master mode, 1bit
- 1-wire data bit with speed up to 24M bps
- Support 8bit/16bit mode
- Separate data input and output bit
- Configurable FIFO size up to 8x16bit for both TX and RX channel
- Support DMA access for TX and RX FIFO

2.9.2. UART

- Up to 4 sets of UART controller
- 2 Support 2-wire mode
- 2 Support 4-wire mode (HW flow control with CTS/RTS)

- Separate up to 256Byte of TX and 384Byte of RX FIFOs
- Programmable FIFO disabling for 1-byte depth
- Programmable baud rate generator supports up to 3Mbps
- Support DMA access for TX and RX channel
- Standard asynchronous communication bits (start, stop and parity).
- Independent masking of transmit FIFO, receive FIFO, receive timeout, modem status, and error condition interrupts.
- False start bit detection
- Line break generation and detection
- Programmable hardware flow control
- Fully-programmable serial interface characteristics
- Support 115200 baud rate

2.9.3. I2C

- 4 sets of I2C controller: 3 sets of master and 1 set of slave
- Compatible with Philips I2C standard
- Support Multi Master Operation
- Software programmable clock frequency
- Clock Stretching and Wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Arbitration lost interrupt, with automatic transfer cancellation
- Start/Stop/Repeated Start/Acknowledge generation
- Start/Stop/Repeated Start detection
- Bus busy detection
- Supports 7 and 10bit addressing mode
- Operates from a wide range of input clock frequencies
- Support 100KHz/400KHz/1M mode

2.9.4. Timer

- 7 sets of 32-bit general purpose timer with individual maskable interrupts

- Register lock function
- Programmable output frequency

1.1.1 WDT

- 32 bits down counter
- Non-Maskable Interrupt (NMI) or WDOG reset
- Optional automatic WDOG reset if NMI handler fails to update the Watchdog register
- Maskable Watchdog freeze by user program
- Configurable clock source

2.9.5. Temp Sensor

- ±3°C untrimmed accuracy (-40ºC to 100ºC)
- ±1.0°C trimmed accuracy (0ºC to 70ºC)
- ±1.25°C trimmed accuracy (-40ºC to 125ºC)
- Calibration sequence requires no knowledge of die temperature
- Digital interface, 12bit resolution

2.9.6. PLL

- Dual power supply: 1.8V (analog)/0.9V(digital) allows for excellent supply noise rejection
- Output frequency range from 360MHz to 1.8GHz
- Duty cycle 50%±2%

2.9.7. INTC

- 2 INTC that support total 4 set of 32-bit source interrupt input
- Support separate interrupt with programmable type (level, edge) and polarity
- Software interrupt control

2.9.8. PWM

- 32-bit counter/timer facility
- single-run or continues run of PTC counter
- Programmable PWM mode

- System clock and external clock sources for timer functionality
- HI/LO Reference and Capture registers
- Three-state control for PWM output driver
- PWM/Timer/Counter functionalities can cause an interrupt to the CPU

2.9.9. Programmable Signals

There are two sets of programmable signal pins referred to as GPIOs and FUNC_SHAREs. A large number of signals, under the control of a programmable register, can be multiplexed on to these pins.

GPIO

- Supports up to 64 GPIOs.
- Programmable modes available to provide selected signals on these pins.
- Individually programmable input/output pins. Defaults to output at reset.
- Each GPIO has a dedicated control signal.
- Supports separate interrupt with programmable type (level, edge) and polarity
- All GPIO pins are also multiplexed on the functionally shared pins.

Functionally Shared Pins

- Supports up to 142 functionally shared signal pins.
- Programmable modes available to provide selected signals on these pins which includes proving the GPIO signals.
- Individually programmable input/output pins, default to output at reset.
- Each functionally shared pin has a dedicated control signal.

3. IP Blocks Supplier List

Table 3-1 IP Blocks Supplier List

S.No.	Name in Specification	Function	Vendor Specific Name	Vendor	IP Version	Comments	Documentation Link
1	VP6	Vision Computing Processor	VP6	Cadence	LX7.1.2		
2	CSI-2 Rx Controller	Camera Serial Interface - receiver	MIPI_CSI2_RX	Cadence	V1.3		MIPI_CSI2_1v3_RX_Controller_User_Guide_v1p15.pdf
3	CSI-2 TX Controller	Camera Serial Interface – transmitter	MIPI_CSI2_RX	Cadence	V1.3		MIPI_CSI2TX_v1.3_User_Guide_v1p08
4	MIPI DSI TX	MIPI Display TX controller	MIPI_DSI_Host_controller	Cadence	V1.3.1		MIPI_DSI_v1.3.1_Host_Controller_User_Guide_v1p09
5	USB 2.0/3.0 controller	USB controller	USB3.0 DRD Controller	Cadence	V1.0		Cadence USB 3 0 DRD Controller - Design Specification.pdf
6	Video Decoder	Video Decoder	Wave511	Chips&Media	V1.10.9		cnm-wave511-datasheet-SiFive_v1.8.0.pdf cnm-wave511-verification_guide-SiFive_v1.9.0.pdf
7	Video Encoder	Video Encoder	Wave521	Chips&Media	V1.18.22		cnm-wave521l-datasheet-SiFive_v1.1.0.pdf cnm-wave521l-verification_guide-SiFive_v1.1.0.pdf
8	JPEG	JPEG Encoder & Decoder	CODAJ12V	Chips&Media	V3.5.6		cnm-codaj12v-datasheet-confidential_v1.4.0.pdf cnm-codaj12-errata-customer_v1.3.0.pdf
9	NNE50	Neutral Network Engine	NNE50	Starfive			
10	VAD	Voice Activity Detector	VAD	Starfive			
11	ISP	Image Signal Processor	ISP	Starfive			
12	CHIPLINK	Serialized Chip-to-Chip Coherent TileLink Interconnect	CHIPLINK	Starfive			
13	PDM	PDM Controller for Digital microphones	PDM	Starfive			
14	PWMDAC	PWM Controller for Digital microphones	PWM	Starfive			
15	Timer	General Purpose Timers		Starfive			
16	WDT	Watch Dog Timer		Starfive			
17	GPIO controller	GPIO Full mux controller		Starfive			
18	PWM	PWM timers		Starfive			

S.No.	Name in Specification	Function	Vendor Specific Name	Vendor	IP Version	Comments	Documentation Link
19	DLA	Deep Learning Accelerator	NVLDA	NVDIA			NVDLA Index of Documentation
20	DDR Controller	Supports DDR4/LPDDR4 DRAMs	ORBIT Memory Controller	OPENEDGES Technology	V1.4		

4. System Application Diagram

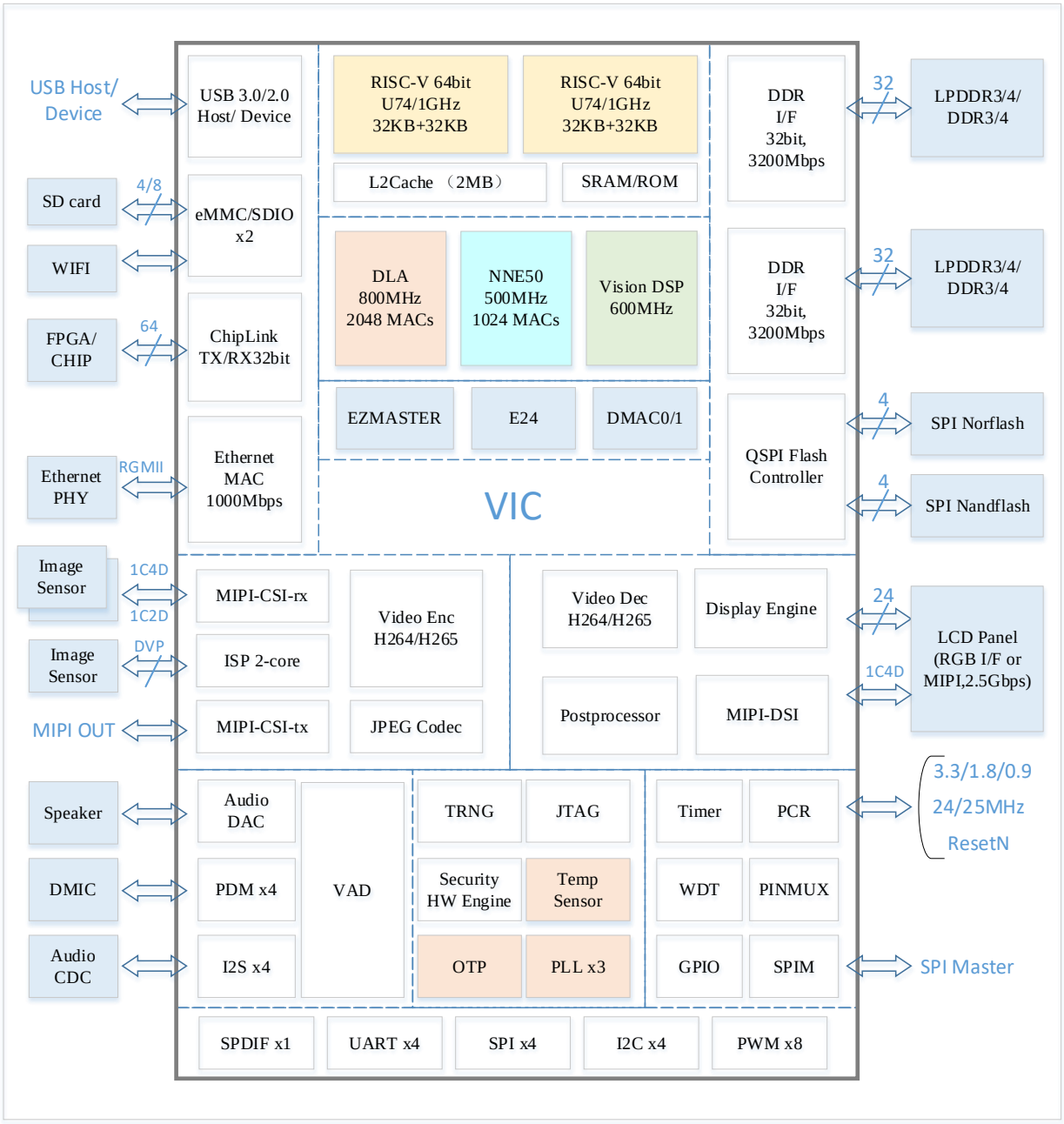


Figure 4-1 Full Feature Application

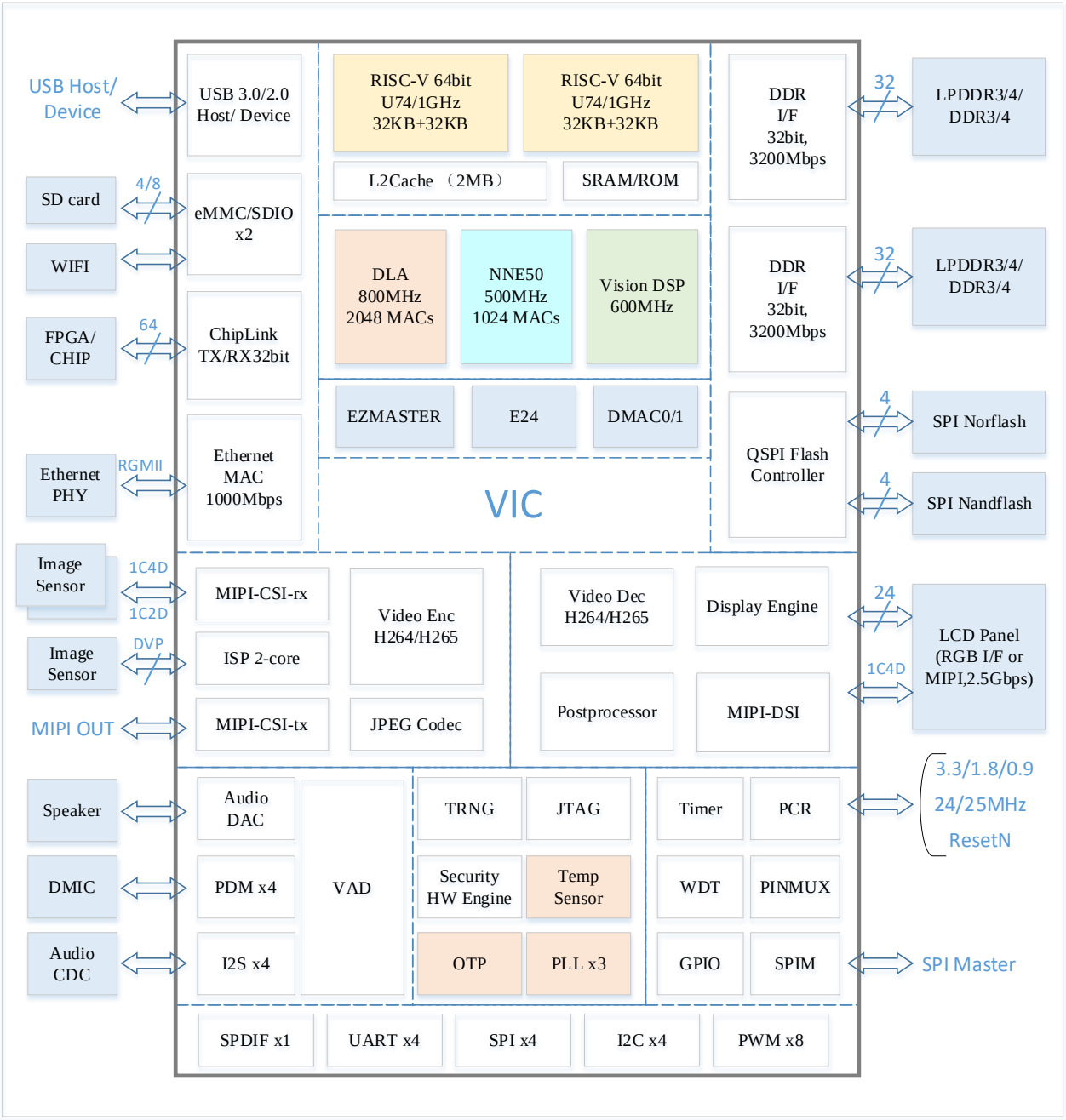


Figure 4-2 USB/Network AI Video Application

4.1. Other Applications

Diagrams for the following applications are TBD.

- AI Enabled Multimedia AP
- Smart Camera Application
- Smart AV Application

5. Functional Block Diagram

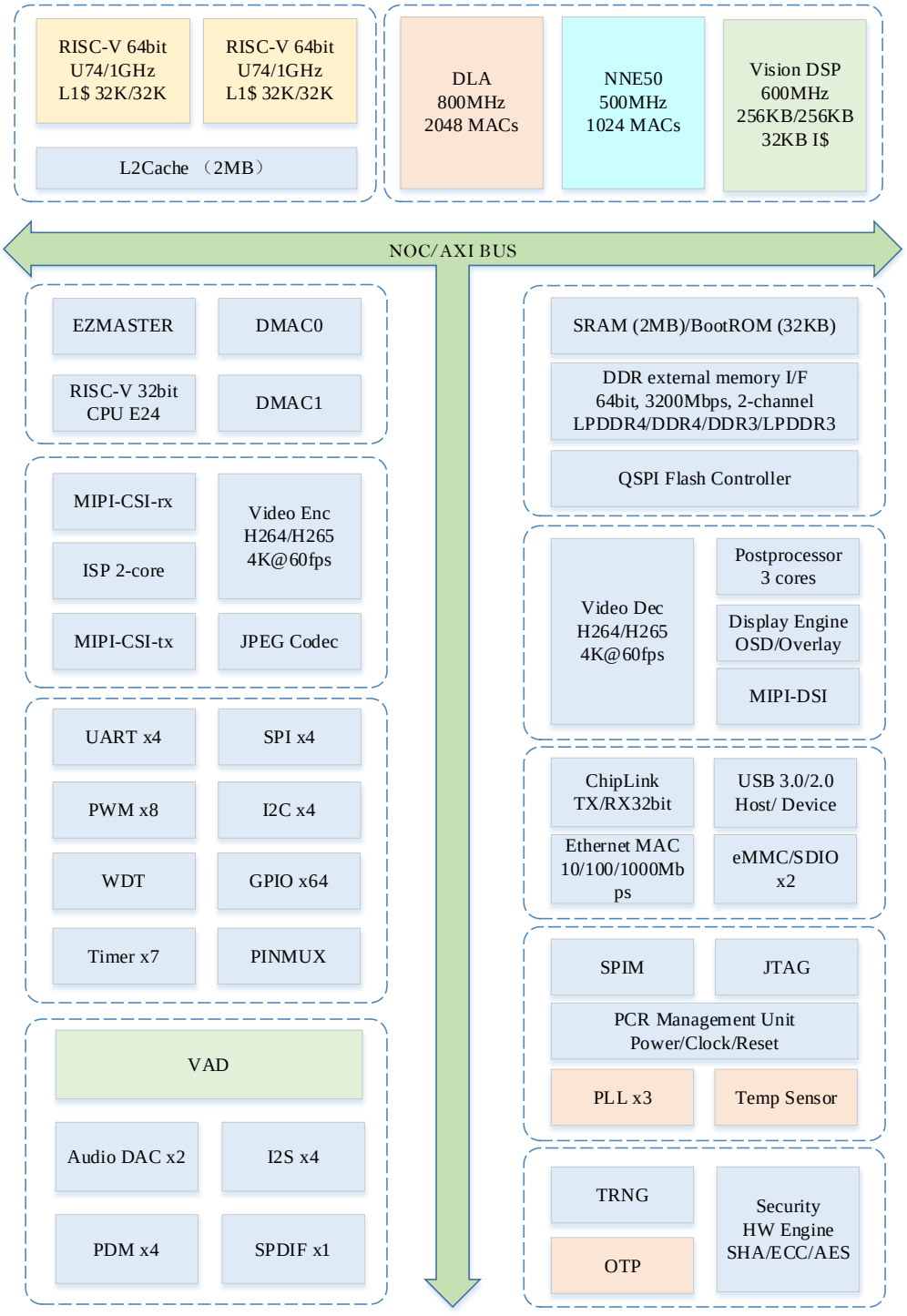


Figure 5-1 Function Block Diagram

6. Memory Map

Table 6-1 U74-MC Memory Map

Start Address	End Address	Size	Attribute	Usage	Notes
0x00_0000_0000	0x00_0000_0FFF		RWX A[1]	Debug	U74 Core
0x00_0000_1000	0x00_01FF_FFFF			Reserved	U74 Core
0x00_0200_0000	0x00_0200_FFFF		RW A	CLINT	U74 Core
0x00_0201_0000	0x00_0201_0FFF		RW A	Cache Controller	U74 Core
0x00_0201_1000	0x00_07FF_FFFF			Reserved	U74 Core
0x00_0800_0000	0x00_081F_FFFF		RWX A	L2 LIM	U74 Core
0x00_0820_0000	0x00_0BFF_FFFF			Reserved	U74 Core
0x00_0C00_0000	0x00_0FFF_FFFF		RW A	PLIC	U74 Core
0x00_1000_0000	0x00_17FF_FFFF	128MB	RW A	peripherals CSR	U74 Core
0x00_1800_0000	0x00_1FFF_FFFF	128MB	RWX	Internal RAM + ROM + slv	Internal ROM, Slave in system 0. 0x1800_0000 - 0x1801_FFFF, intRAM0 1. 0x1808_0000 - 0x1809_FFFF, intRAM1 2. 0x1840_0000 - 0x1840_7FFF, ROM 3. 0x1900_0000 - 0x193F_FFFF, reserved 4. 0x1940_0000 - 0x195F_FFFF, reserved 5. 0x1960_0000 - 0x197F_FFFF, NNE slave 6. 0x1980_0000 - 0x19BF_FFFF, ISP slave 7. 0x19C0_0000 - 0x19FF_FFFF, DLA slave
0x00_2000_0000	0x00_3FFF_FFFF	256MB	RWX	QSPI	off-chip QSPI NOR/NAND flash, belong to VIC
0x00_4000_0000	0x00_40FF_FFFF	16MB	RWX	VP6 slv	
0x00_4100_0000	0x00_5FFF_FFFF	496MB	RWX	ChipLink	Non-cacheable space. Remapped to 0x00_6100_0000 - 0x00_7FFF_FFFF
0x10_0000_0000	0x17_FFFF_FFFF	32GB	RWX	DDR	Off-chip DDR, belong to VIC, non-cacheable. remapped to 0x00_8000_0000 - 0x08_7FFF_FFFF
0x20_0000_0000	0x2F_FFFF_FFFF	64GB	RWX	ChipLink	ChipLink, non-cacheable space, remapped to 0x30_0000_0000 - 0x3F_FFFF_FFFF
0x00_6100_0000	0x00_7FFF_FFFF	496MB	RWX C A	ChipLink	ChipLink, cacheable, the same physical memory with system port 0x00_4000_0000 - 0x00_5000_0000 space
0x00_8000_0000	0x08_7FFF_FFFF	32GB	RWX C A	DDR	Off-chip DDR, belong to VIC, the same physical memory with system port 0x00_8000_0000 - 0x08_7000_0000 space
0x30_0000_0000	0x3F_FFFF_FFFF	64GB	RWX C A	ChipLink	ChipLink, cacheable, the same physical memory with system port 0x20_0000_0000 - 0x2F_0000_0000 space

[1] Memory attributes: **R** - Read, **W** -Write, **X** - Execute, **C** - Cacheable, **A** - Atomics

Table 6-2 Peripherals Port Memory Map

Peripherals Port	Start Address	End Address	Size
SDIO0_CSR	0x00_1000_0000	0x00_1000_FFFF	64KB
SDIO1_CSR	0x00_1001_0000	0x00_1001_FFFF	64KB
GMAC_CSR	0x00_1002_0000	0x00_1002_FFFF	64KB
EZMASTER_CSR	0x00_1003_0000	0x00_100A_FFFF	512KB
SGDMA2P_CSR	0x00_100B_0000	0x00_100B_FFFF	64KB
RESERVED	0x00_100C_0000	0x00_100C_FFFF	
SECENGINE	0x00_100D_0000	0x00_100E_FFFF	128KB
SPI2AHB_CSR	0x00_100F_0000	0x00_100F_FFFF	64KB
GPU2D_CSR	0x00_1010_0000	0x00_1013_FFFF	256KB
RESERVED	0x00_1014_0000	0x00_103F_FFFF	
I2SADC	0x00_1040_0000	0x00_1040_FFFF	64KB
PDM	0x00_1041_0000	0x00_1041_FFFF	64KB
VAD	0x00_1042_0000	0x00_1042_FFFF	64KB
SPDIF	0x00_1043_0000	0x00_1043_FFFF	64KB
PWMDAC	0x00_1044_0000	0x00_1044_FFFF	64KB
I2SDAC0	0x00_1045_0000	0x00_1045_FFFF	64KB
I2SDAC1	0x00_1046_0000	0x00_1046_FFFF	64KB
I2SDAC16K	0x00_1047_0000	0x00_1047_FFFF	64KB
DOM_AUDIO_CLKGEN	0x00_1048_0000	0x00_1048_FFFF	64KB
DOM_AUDIO_RSTGEN	0x00_1049_0000	0x00_1049_FFFF	64KB
DOM_AUDIO_SYSCTRL	0x00_104A_0000	0x00_104A_FFFF	64KB
USB	0x00_104C_0000	0x00_104F_FFFF	256KB
SGDMA1P	0x00_1050_0000	0x00_1050_FFFF	64KB
NNE_CSR	0x00_1080_0000	0x00_108F_FFFF	1MB
RESERVED	0x00_1090_0000	0x00_10FF_FFFF	4MB
NOC_CSR	0x00_1100_0000	0x00_117F_FFFF	8MB
CLKGEN_CSR	0x00_1180_0000	0x00_1180_FFFF	64KB
OTP	0x00_1181_0000	0x00_1181_FFFF	64KB
DDRPHY0_CSR	0x00_1182_0000	0x00_1182_FFFF	64KB
DDRPHY1_CSR	0x00_1183_0000	0x00_1183_FFFF	64KB
RSTGEN_CSR	0x00_1184_0000	0x00_1184_FFFF	64KB

Peripherals Port	Start Address	End Address	Size
SYSCTRL-MAINSYS	0x00_1185_0000	0x00_1185_3FFF	16KB
SYSCTRL-REMAP_VP6NOC	0x00_1185_4000	0x00_1185_7FFF	16KB
SYSCTRL-IOPAD_CTRL	0x00_1185_8000	0x00_1185_BFFF	16KB
SYSCTRL_SIMU_TEST	0x00_1185_C000	0x00_1185_FFFF	16KB
QSPI_CSR	0x00_1186_0000	0x00_1186_FFFF	64KB
HSUART0	0x00_1187_0000	0x00_1187_FFFF	64KB
HSUART1	0x00_1188_0000	0x00_1188_FFFF	64KB
SPI0	0x00_1189_0000	0x00_1189_FFFF	64KB
SPI1	0x00_118A_0000	0x00_118A_FFFF	64KB
I2C0	0x00_118B_0000	0x00_118B_FFFF	64KB
I2C1	0x00_118C_0000	0x00_118C_FFFF	64KB
TRNG	0x00_118D_0000	0x00_118D_FFFF	64KB
VENC_CSR	0x00_118E_0000	0x00_118E_EFFF	64KB
VDEC_CSR	0x00_118F_0000	0x00_118F_EFFF	64KB
JPEG_CSR	0x00_1190_0000	0x00_1190_FFFF	64KB
GPIO	0x00_1191_0000	0x00_1191_FFFF	64KB
DLA_CSR	0x00_1194_0000	0x00_1197_FFFF	256KB
VP6_APB	0x00_11A0_0000	0x00_11AF_FFFF	1MB
RESERVED	0x00_11B0_0000	0x00_11FF_FFFF	
LCDC	0x00_1200_0000	0x00_1200_FFFF	64KB
VPP0	0x00_1204_0000	0x00_1204_FFFF	64KB
VPP1	0x00_1208_0000	0x00_1208_FFFF	64KB
DSITX	0x00_1210_0000	0x00_1210_FFFF	64KB
VPP2	0x00_120c_0000	0x00_120c_FFFF	64KB
PIXRAWOUT	0x00_1220_0000	0x00_1220_FFFF	64KB
MAP_CONVERTER	0x00_1221_0000	0x00_1221_FFFF	64KB
CSI2TX	0x00_1222_0000	0x00_1222_FFFF	64KB
VOUT_CLKGEN	0x00_1224_0000	0x00_1224_FFFF	64KB
VOUT_RSTGEN	0x00_1225_0000	0x00_1225_FFFF	64KB
VOUT_SYSCON	0x00_1226_0000	0x00_1226_FFFF	64KB
VP6_INTC0	0x00_1240_0000	0x00_1240_FFFF	64KB
SPI2	0x00_1241_0000	0x00_1241_FFFF	64KB

Peripherals Port	Start Address	End Address	Size
SPI3	0x00_1242_0000	0x00_1242_FFFF	64KB
UART2	0x00_1243_0000	0x00_1243_FFFF	64KB
UART3	0x00_1244_0000	0x00_1244_FFFF	64KB
I2C2	0x00_1245_0000	0x00_1245_FFFF	64KB
I2C3	0x00_1246_0000	0x00_1246_FFFF	64KB
CHIPLINK/MSI SLAVE	0x00_1247_0000	0x00_1247_7FFF	32KB
CHIPLINK/ERROR_DEVICE	0x00_1247_8000	0x00_1247_FFFF	32KB
WDT	0x00_1248_0000	0x00_1248_FFFF	64KB
PWM	0x00_1249_0000	0x00_1249_FFFF	64KB
TEMPSENSOR	0x00_124A_0000	0x00_124A_FFFF	64KB
VP6_INTC1	0x00_124B_0000	0x00_124B_FFFF	64KB
SYS_ERRDEV_CSR	0x00_124C_0000	0x00_124C_FFFF	64KB
RESERVED (ILLEGAL)	0x00_124D_0000	0x00_17FF_FFFF	

7. System Boot Method and Sequence

7.1. Boot Source

Table 7-1 Boot Source

Processor	SCFG_boot_mode [default: 0x0]	PAD_GPIO[63] (Boot source sel)	Boot Vector	PAD_GPIO[62:60] (Loader location determined)	Notes
U74	0x1	don't care	SCFG_u74_reset_vector, configured through syscon		1. Default use IO Pad to sel the boot vector and loader source, so SCFG_boot_mode default 1'b0 2. SCFG_u74_reset_vector be configurable by SPI2AHB 3. PAD_GPIO[63] and PAD_GPIO[62:60] determined thru the pull-up or pull-down on board.
	0x0	0x0	0x00_2000_0000, XIP Flash	0x0: Boot from 1bit QSPI nor flash 0x1: Boot from 4bit QSPI nor flash 0x2: Reserved 0x3: Reserved 0x4: Boot from UART 0x5: Reserved 0x6: Reserved 0x7: SPI2AHB	
		0x1	0x00_1840_0000, on-chip boot ROM (32KB)		
VP6	N/A		configurable by U74 or E24		
Note: The boot mode and boot sel can be read thru syscon status registers					

7.2. Boot Sequence

Table 7-2 Boot Sequence

Processor	Stage	Description	Notes
U74	Power on	power on the system	
	Clkgen and Release U74	1. Clkgen for CPU and peripherals 2. Release the u74's reset 3. keep VP6 and ADSP's in reset state	
	U74 Boot	1. U74 boot from memory according to the boot address	
VP6	Config rstVec	1. U74 config the reset vector into syscon, and the vector output to DSP 2. reset the DSP thru config the reset CSR of DSP if DSP need boot again	It needs remap the address if DSP's reset vector fixed
	Release Core	Release the reset of DSP	
	Boot	DSP boot from the address according to the configuration	

8. Clock & Reset

8.1. Clock Source

- Two external oscillator OSC0 and OSC1 input

  OSC0 25M default for USB, GMAC and system main clock source

  OSC1 input 12-27MHz according to application

- Three PLLs

  PLL0 used for system main logic, including CPU, bus

  PLL1 output to support DDR, DLA and DSP

  PLL2 output to support slow speed peripherals, video input and video output

8.2. Reset

pad_rstn is an asynchronous active low reset that can be connected to a external reset device output. There is not internal de-bounce logic.

rst_pll, rstn_clkgen, rstn_sys are generated by internal synchronous resets for respective clock domains.

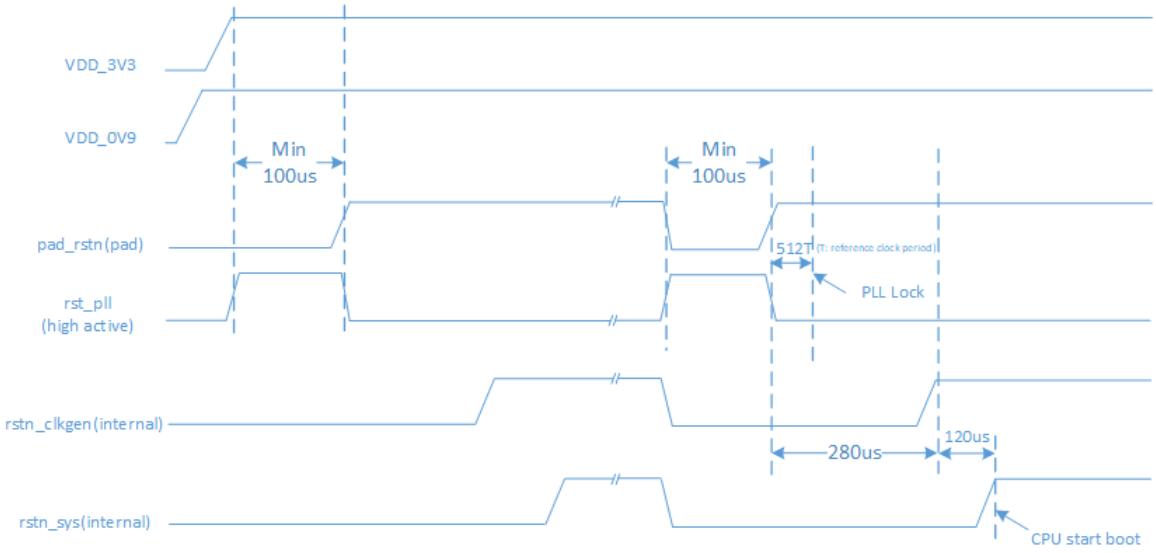


Figure 8-1 Reset timing

9. Chip Power On/Off Sequence

- Power-up/down sequence

No limitation for core VDD power-up/down sequence: VDD can be powered on/off first or last.

- Power-up

First power up 1.8V by external 1.8V system power through PVDD18RGM; after at least 20us, power up 3.3V through PVDD3RGM.

- Power-down

First power down 3.3V through PVDD3RGM; after at least 20us, power down 1.8V system power through PVDD18RGM.

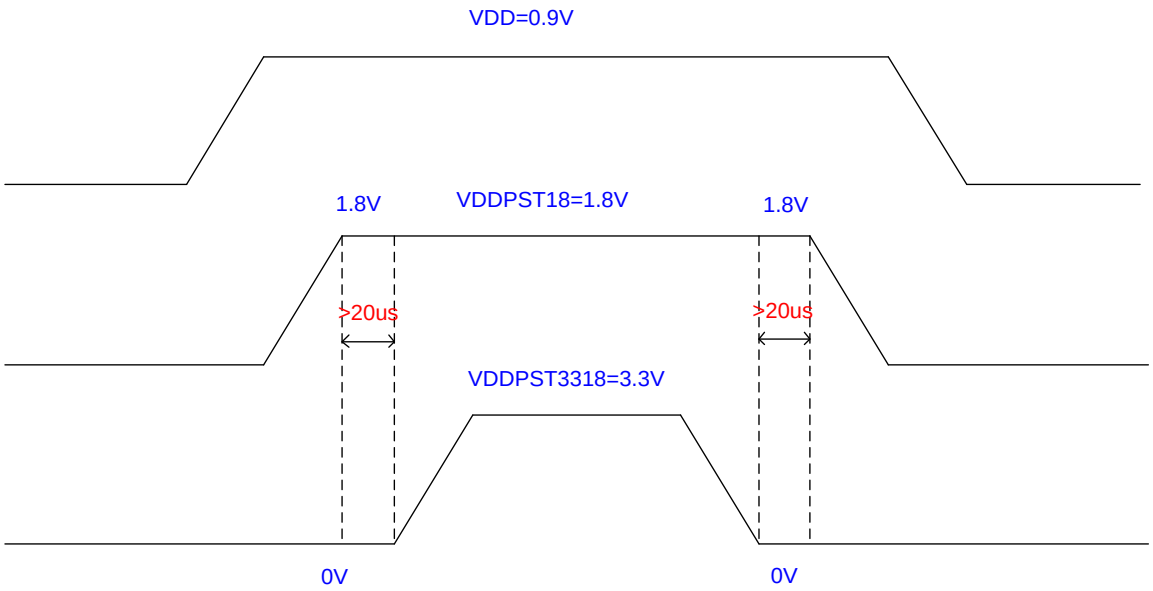


Figure 9-1 Chip Power on/off Sequence

10. Pin list and ball map

10.1. Pin List & Description

Table 10-1 Pin List

Pin Number	Pin Name	IO-Type	Description
A1	DDR0_DQ[30]	DDR	DDR SDRAM0 data [30]
A2	DDR0_DQ[24]	DDR	DDR SDRAM0 data [24]
A3	DDR0_DQ[26]	DDR	DDR SDRAM0 data [26]
A4	VSS	VSS	Digital ground
A5	DDR0_DQ[16]	DDR	DDR SDRAM0 data [16]
A6	DDR0_DQS_P[2]	DDR	DDR SDRAM0 Data Strobe DQS2_P
A7	VSS	VSS	Digital ground
A9	DDR0_ACT_N	DDR	DDR SDRAM0 ACT_n
A10	DDR0_ADR[11]	DDR	DDR SDRAM0 Address [11]
A11	VSS	VSS	Digital ground
A12	DDR0_CK_P[1]	DDR	DDR SDRAM0 differential clock inputs CK1_P
A14	DDR0_CK_P[0]	DDR	DDR SDRAM0 differential clock inputs CK0_P
A15	DDR0_ADR[2]	DDR	DDR SDRAM0 Address [2]
A16	DDR0_ATB0	DDR	DDR0 PHY IO pad Analog Test Bus (ATB)
A17	DDR0_CS_N[1]	DDR	DDR SDRAM0 CS1
A18	VSS	VSS	Digital ground
A19	DDR0_DQ[15]	DDR	DDR SDRAM0 data [15]
A20	DDR0_DQS_N[1]	DDR	DDR SDRAM0 Data Strobe DQS1_N
A21	DDR0_DQ[8]	DDR	DDR SDRAM0 data [8]
A22	DDR0_DQ[7]	DDR	DDR SDRAM0 data [7]
A23	DDR0_DQ[6]	DDR	DDR SDRAM0 data [6]
A25	GPIO[0]	IO	function IO share with GPIO
A26	GPIO[3]	IO	function IO share with GPIO
A27	GPIO[6]	IO	function IO share with GPIO
A28	GPIO[9]	IO	function IO share with GPIO
A29	GPIO[12]	IO	function IO share with GPIO
A30	GPIO[15]	IO	function IO share with GPIO
A31	GPIO[17]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
AA1	FUNC_SHARE[72]	IO	function IO share with group
AA2	FUNC_SHARE[77]	IO	function IO share with group
AA3	FUNC_SHARE[70]	IO	function IO share with group
AA4	FUNC_SHARE[71]	IO	function IO share with group
AA5	FUNC_SHARE[74]	IO	function IO share with group
AA6	FUNC_SHARE[75]	IO	function IO share with group
AA8	VSS	VSS	Digital ground
AA9	VDD3318_SENSOR	VDD3318	FUNC_SHARE[98-114] IO power
AA10	VSS	VSS	Digital ground
AA11	VDD	VDD	digital core power
AA12	VSS	VSS	Digital ground
AA13	VSS	VSS	Digital ground
AA14	VSS	VSS	Digital ground
AA15	VSS	VSS	Digital ground
AA16	VDDQCK_DDR1	DDR	DDR CK power
AA17	VSS	VSS	Digital ground
AA18	VDDPLL_DDR1	DDR	DDR PLL power
AA19	VSS	VSS	Digital ground
AA20	VSS	VSS	Digital ground
AA21	VDD3318_GMII	VDD3318	FUNC_SHARE[115-141] IO power
AA22	VSS	VSS	Digital ground
AA23	AVDD33_USB	AVDD33	USB analog power supply
AA24	AVSS_USB	AVSS	USB analog ground
AA25	FUNC_SHARE[121]	IO	function IO share with group
AA26	FUNC_SHARE[120]	IO	function IO share with group
AA27	FUNC_SHARE[115]	IO	function IO share with group
AA28	FUNC_SHARE[124]	IO	function IO share with group
AA29	VSS	VSS	Digital ground
AA30	FUNC_SHARE[125]	IO	function IO share with group
AA31	FUNC_SHARE[128]	IO	function IO share with group
AB1	FUNC_SHARE[76]	IO	function IO share with group
AB2	FUNC_SHARE[81]	IO	function IO share with group
AB3	VSS	VSS	Digital ground
AB4	FUNC_SHARE[85]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
AB5	FUNC_SHARE[78]	IO	function IO share with group
AB6	FUNC_SHARE[79]	IO	function IO share with group
AB7	FUNC_SHARE[82]	IO	function IO share with group
AB8	VSS	VSS	Digital ground
AB9	VDD3318_SENSOR	VDD3318	FUNC_SHARE[98-114] IO power
AB10	VSS	VSS	Digital ground
AB11	VSS	VSS	Digital ground
AB12	VDDQ_DDR1	DDR	DDR IO power
AB13	VDDQ_DDR1	DDR	DDR IO power
AB14	VDDQ_DDR1	DDR	DDR IO power
AB15	VDDQ_DDR1	DDR	DDR IO power
AB16	VDDQ_DDR1	DDR	DDR IO power
AB17	VSS	VSS	Digital ground
AB18	VDDQ_DDR1	DDR	DDR IO power
AB19	VSS	VSS	Digital ground
AB20	VSS	VSS	Digital ground
AB21	DVDD18_OTP	DVDD18	OTP power
AB22	VSS18_OTP	VSS	OTP ground
AB30	FUNC_SHARE[117]	IO	function IO share with group
AB31	FUNC_SHARE[119]	IO	function IO share with group
AC1	FUNC_SHARE[80]	IO	function IO share with group
AC8	VSS	VSS	Digital ground
AC9	VSS	VSS	Digital ground
AC10	VSS	VSS	Digital ground
AC11	VDDQ_DDR1	DDR	DDR IO power
AC12	VDDQ_DDR1	DDR	DDR IO power
AC13	VDDQ_DDR1	DDR	DDR IO power
AC14	VSS	VSS	Digital ground
AC15	VSS	VSS	Digital ground
AC16	VDDQ_DDR1	DDR	DDR IO power
AC17	VSS	VSS	Digital ground
AC18	VDDQ_DDR1	DDR	DDR IO power
AC19	VSS	VSS	Digital ground
AC20	VSS	VSS	Digital ground

Pin Number	Pin Name	IO-Type	Description
AC21	ANA18_OTP_PENVDD2	ANA18	OTP VDD2 power enable flag
AC22	VSS	VSS	Digital ground
AC23	AVDD09TX_USB	AVDD	USB TX analog power
AC24	AVSSTX_USB	AVSS	USB TX analog ground
AC25	VSS	VSS	Digital ground
AC26	USB_SSTXB1	USB	USB 3.0 TX P signal
AC27	USB_SSTXA1	USB	USB 3.0 TX P signal
AC28	USB_DP	USB	USB 2.0 DP
AC29	USB_DM	USB	USB 2.0 DM
AC30	USB_SSRXB2	USB	USB 3.0 RX M signal
AC31	USB_SSRXA2	USB	USB 3.0 RX P signal
AD1	FUNC_SHARE[84]	IO	function IO share with group
AD2	FUNC_SHARE[89]	IO	function IO share with group
AD3	FUNC_SHARE[92]	IO	function IO share with group
AD4	FUNC_SHARE[96]	IO	function IO share with group
AD5	FUNC_SHARE[97]	IO	function IO share with group
AD6	FUNC_SHARE[102]	IO	function IO share with group
AD7	FUNC_SHARE[101]	IO	function IO share with group
AD8	VDDQ_DDR1	DDR	DDR IO power
AD9	VDDQ_DDR1	DDR	DDR IO power
AD10	VDDQ_DDR1	DDR	DDR IO power
AD11	VDDQ_DDR1	DDR	DDR IO power
AD12	VDDQ_DDR1	DDR	DDR IO power
AD13	VSS	VSS	Digital ground
AD14	VSS	VSS	Digital ground
AD15	VSS	VSS	Digital ground
AD16	VDDQ_DDR1	DDR	DDR IO power
AD17	VDDQ_DDR1	DDR	DDR IO power
AD18	VDDQ_DDR1	DDR	DDR IO power
AD19	VSS	VSS	Digital ground
AD20	VSS	VSS	Digital ground
AD21	VSS	VSS	Digital ground
AD22	VSS	VSS	Digital ground
AD23	AVDD09RX_USB	AVDD	USB RX analog power

Pin Number	Pin Name	IO-Type	Description
AD24	AVDD18_USB	AVDD18	USB analog power
AD25	VSS	VSS	Digital ground
AD26	USB_SSRXB1	USB	USB 3.0 RX M signal
AD27	USB_SSRXA1	USB	USB 3.0 RX P signal
AD28	VSS	VSS	Digital ground
AD29	VSS	VSS	Digital ground
AD30	USB_SSTXA2	USB	USB 3.0 TX P signal
AD31	USB_SSTXB2	USB	USB 3.0 TX P signal
AE1	FUNC_SHARE[88]	IO	function IO share with group
AE2	FUNC_SHARE[93]	IO	function IO share with group
AE3	VSS	VSS	Digital ground
AE4	FUNC_SHARE[94]	IO	function IO share with group
AE5	FUNC_SHARE[104]	IO	function IO share with group
AE6	FUNC_SHARE[108]	IO	function IO share with group
AE7	FUNC_SHARE[112]	IO	function IO share with group
AE8	VSS	VSS	Digital ground
AE9	VDDQ_DDR1	DDR	DDR IO power
AE10	VDDQ_DDR1	DDR	DDR IO power
AE11	VSS	VSS	Digital ground
AE12	VDDQ_DDR1	DDR	DDR IO power
AE13	DDR1_ADR[9]	DDR	DDR SDRAM1 Address [9]
AE14	VSS	VSS	Digital ground
AE15	VSS	VSS	Digital ground
AE16	DDR1_BG[0]	DDR	DDR SDRAM1 Bank Group0
AE17	VDDQ_DDR1	DDR	DDR IO power
AE18	DDR1_CAS_N_ADR15	DDR	DDR SDRAM1 Address 15
AE19	VDDQ_DDR1	DDR	DDR IO power
AE20	VSS	VSS	Digital ground
AE21	VDDQ_DDR1	DDR	DDR IO power
AE22	VDDQ_DDR1	DDR	DDR IO power
AE23	AVSSRX_USB	AVSS	USB RX analog ground
AE24	VSS	VSS	Digital ground
AE31	VSS	VSS	Digital ground
AF1	FUNC_SHARE[99]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
AF7	DDR1_DQ[31]	DDR	DDR SDRAM1 data [31]
AF8	DDR1_DQ[28]	DDR	DDR SDRAM1 data [28]
AF10	DDR1_DQ[23]	DDR	DDR SDRAM1 data [23]
AF11	DDR1_DQ[22]	DDR	DDR SDRAM1 data [22]
AF13	DDR1_ADR[6]	DDR	DDR SDRAM1 Address [6]
AF14	DDR1_ADR[3]	DDR	DDR SDRAM1 Address [3]
AF16	DDR1_BA[1]	DDR	DDR SDRAM1 Bank Address 1
AF18	DDR1_WE_N_ADR14	DDR	DDR SDRAM1 Address 14
AF20	DDR1_CS_N[3]	DDR	DDR SDRAM1 CS3
AF21	DDR1_PLL_REFOUT_N	DDR	DDR1 PHY Differential PLL reference clock output
AF23	DDR1_DQ[15]	DDR	DDR SDRAM1 data [15]
AF24	DDR1_DQ[14]	DDR	DDR SDRAM1 data [14]
AF26	DDR1_DQ[8]	DDR	DDR SDRAM1 data [8]
AF27	VSS	VSS	Digital ground
AF29	DDR1_DQ[0]	DDR	DDR SDRAM1 data [0]
AF30	DDR1_DQ[3]	DDR	DDR SDRAM1 data [3]
AG1	FUNC_SHARE[100]	IO	function IO share with group
AG2	FUNC_SHARE[83]	IO	function IO share with group
AG3	FUNC_SHARE[87]	IO	function IO share with group
AG4	FUNC_SHARE[91]	IO	function IO share with group
AG5	VSS	VSS	Digital ground
AG7	DDR1_DQ[30]	DDR	DDR SDRAM1 data [30]
AG8	DDR1_DQ[29]	DDR	DDR SDRAM1 data [29]
AG10	DDR1_DQ[20]	DDR	DDR SDRAM1 data [20]
AG11	DDR1_DM_DBI_N[2]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AG14	DDR1_ADR[5]	DDR	DDR SDRAM1 Address [5]
AG16	DDR1_ADR[0]	DDR	DDR SDRAM1 Address [0]
AG18	VSS	VSS	Digital ground
AG20	DDR1_CAL	DDR	DDR1 PHY IO pad calibration resistor connection
AG21	DDR1_PLL_REFOUT_P	DDR	DDR1 PHY Differential PLL reference clock output
AG23	DDR1_CKE[0]	DDR	DDR SDRAM1 Clock0 enable
AG24	VSS	VSS	Digital ground
AG26	DDR1_DQ[11]	DDR	DDR SDRAM1 data [11]

Pin Number	Pin Name	IO-Type	Description
AG27	DDR1_DQ[10]	DDR	DDR SDRAM1 data [10]
AG29	DDR1_DQ[1]	DDR	DDR SDRAM1 data [1]
AG30	DDR1_DM_DBI_N[0]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AH1	FUNC_SHARE[103]	IO	function IO share with group
AH2	FUNC_SHARE[86]	IO	function IO share with group
AH3	VSS	VSS	Digital ground
AH4	FUNC_SHARE[95]	IO	function IO share with group
AH5	FUNC_SHARE[106]	IO	function IO share with group
AH7	VSS	VSS	Digital ground
AH8	DDR1_DM_DBI_N[3]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AH10	VSS	VSS	Digital ground
AH11	DDR1_DQ[21]	DDR	DDR SDRAM1 data [21]
AH13	VSS	VSS	Digital ground
AH14	DDR1_ADR[7]	DDR	DDR SDRAM1 Address [7]
AH16	VSS	VSS	Digital ground
AH18	DDR1_PAR	DDR	DDR SDRAM1 PAR0
AH20	DDR1_CS_N[2]	DDR	DDR SDRAM1 CS2
AH21	DDR1_CS_N[1]	DDR	DDR SDRAM1 CS1
AH23	DDR1_ODT[1]	DDR	DDR SDRAM1 On Die Termination for CS1
AH24	DDR1_ODT[0]	DDR	DDR SDRAM1 On Die Termination for CS0
AH26	VSS	VSS	Digital ground
AH27	DDR1_DQ[9]	DDR	DDR SDRAM1 data [9]
AH29	VSS	VSS	Digital ground
AH30	DDR1_DQ[2]	DDR	DDR SDRAM1 data [2]
AJ1	FUNC_SHARE[105]	IO	function IO share with group
AJ7	DDR1_DQS_P[3]	DDR	DDR SDRAM1 Data Strobe DQS3_P
AJ8	DDR1_DQ[27]	DDR	DDR SDRAM1 data [27]
AJ10	DDR1_DQS_N[2]	DDR	DDR SDRAM1 Data Strobe DQS2_N
AJ11	DDR1_DQ[19]	DDR	DDR SDRAM1 data [19]
AJ12	DDR1_BG[1]	DDR	DDR SDRAM1 Bank Group1
AJ13	DDR1_ADR[12]	DDR	DDR SDRAM1 Address [12]
AJ14	DDR1_ADR[10]	DDR	DDR SDRAM1 Address [10]

Pin Number	Pin Name	IO-Type	Description
AJ16	DDR1_ADR[2]	DDR	DDR SDRAM1 Address [2]
AJ18	DDR1_ADR[1]	DDR	DDR SDRAM1 Address [1]
AJ20	DDR1_ERR_N	DDR	DDR SDRAM1 alert_n
AJ21	VSS	VSS	Digital ground
AJ23	VSS	VSS	Digital ground
AJ24	DDR1_CKE[1]	DDR	DDR SDRAM1 Clock1 enable
AJ26	DDR1_DM_DBI_N[1]	DDR	DDR SDRAM1 Input Data Mask and Data Bus Inversion for byte0
AJ27	DDR1_DQS_P[1]	DDR	DDR SDRAM1 Data Strobe DQS1_P
AJ29	DDR1_DQ[4]	DDR	DDR SDRAM1 data [4]
AJ30	DDR1_DQS_N[0]	DDR	DDR SDRAM1 Data Strobe DQS0_N
AK1	FUNC_SHARE[107]	IO	function IO share with group
AK2	FUNC_SHARE[109]	IO	function IO share with group
AK3	VSS	VSS	Digital ground
AK4	FUNC_SHARE[98]	IO	function IO share with group
AK5	VSS	VSS	Digital ground
AK7	DDR1_DQS_N[3]	DDR	DDR SDRAM1 Data Strobe DQS3_N
AK8	DDR1_DQ[26]	DDR	DDR SDRAM1 data [26]
AK10	DDR1_DQS_P[2]	DDR	DDR SDRAM1 Data Strobe DQS2_P
AK11	DDR1_DQ[17]	DDR	DDR SDRAM1 data [17]
AK12	DDR1_ADR[13]	DDR	DDR SDRAM1 Address [13]
AK13	DDR1_ACT_N	DDR	DDR SDRAM1 ACT_n
AK14	DDR1_ADR[8]	DDR	DDR SDRAM1 Address [8]
AK16	DDR1_CK_N[1]	DDR	DDR SDRAM1 differential clock inputs CK1_N
AK18	DDR1_CK_N[0]	DDR	DDR SDRAM1 differential clock inputs CK0_N
AK20	DDR1_RAS_N_ADR16	DDR	DDR SDRAM1 Address 16
AK21	DDR1_ATB0	DDR	DDR1 PHY IO pad Analog Test Bus (ATB)
AK23	DDR1_CS_N[0]	DDR	DDR SDRAM1 CS0
AK24	DDR1_PLL_TESTOUT_N	DDR	DDR1 PHY Differential PLL test clock output
AK26	VSS	VSS	Digital ground
AK27	DDR1_DQS_N[1]	DDR	DDR SDRAM1 Data Strobe DQS1_N
AK29	DDR1_DQ[5]	DDR	DDR SDRAM1 data [5]
AK30	DDR1_DQS_P[0]	DDR	DDR SDRAM1 Data Strobe DQS0_P
AL1	FUNC_SHARE[111]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
AL2	FUNC_SHARE[113]	IO	function IO share with group
AL3	FUNC_SHARE[90]	IO	function IO share with group
AL4	FUNC_SHARE[110]	IO	function IO share with group
AL5	FUNC_SHARE[114]	IO	function IO share with group
AL6	VSS	VSS	Digital ground
AL7	DDR1_DQ[25]	DDR	DDR SDRAM1 data [25]
AL8	DDR1_DQ[24]	DDR	DDR SDRAM1 data [24]
AL9	VSS	VSS	Digital ground
AL10	DDR1_DQ[18]	DDR	DDR SDRAM1 data [18]
AL11	DDR1_DQ[16]	DDR	DDR SDRAM1 data [16]
AL12	VSS	VSS	Digital ground
AL13	DDR1_ADR[11]	DDR	DDR SDRAM1 Address [11]
AL14	DDR1_ADR[4]	DDR	DDR SDRAM1 Address [4]
AL15	VSS	VSS	Digital ground
AL16	DDR1_CK_P[1]	DDR	DDR SDRAM1 differential clock inputs CK1_P
AL18	DDR1_CK_P[0]	DDR	DDR SDRAM1 differential clock inputs CK0_P
AL19	VSS	VSS	Digital ground
AL20	DDR1_BA[0]	DDR	DDR SDRAM1 Bank Address 0
AL21	DDR1_ATB1	DDR	DDR1 PHY IO pad Analog Test Bus (ATB)
AL22	VSS	VSS	Digital ground
AL23	DDR1_RESET_N	DDR	DDR SDRAM1 Active Low Asynchronous Reset
AL24	DDR1_PLL_TESTOUT_P	DDR	DDR1 PHY Differential PLL test clock output
AL25	VSS	VSS	Digital ground
AL26	DDR1_DQ[13]	DDR	DDR SDRAM1 data [13]
AL27	DDR1_DQ[12]	DDR	DDR SDRAM1 data [12]
AL28	VSS	VSS	Digital ground
AL29	DDR1_DQ[7]	DDR	DDR SDRAM1 data [7]
AL30	DDR1_DQ[6]	DDR	DDR SDRAM1 data [6]
B1	DDR0_DQ[29]	DDR	DDR SDRAM0 data [29]
B2	DDR0_DQ[28]	DDR	DDR SDRAM0 data [28]
B3	DDR0_DQ[25]	DDR	DDR SDRAM0 data [25]
B4	DDR0_DQ[23]	DDR	DDR SDRAM0 data [23]
B5	DDR0_DQ[20]	DDR	DDR SDRAM0 data [20]
B6	DDR0_DQS_N[2]	DDR	DDR SDRAM0 Data Strobe DQS2_N

Pin Number	Pin Name	IO-Type	Description
B7	DDR0_ADR[12]	DDR	DDR SDRAM0 Address [12]
B9	DDR0_ADR[6]	DDR	DDR SDRAM0 Address [6]
B10	DDR0_ADR[1]	DDR	DDR SDRAM0 Address [1]
B11	DDR0_ADR[10]	DDR	DDR SDRAM0 Address [10]
B12	DDR0_CK_N[1]	DDR	DDR SDRAM0 differential clock inputs CK1_N
B14	DDR0_CK_N[0]	DDR	DDR SDRAM0 differential clock inputs CK0_N
B15	DDR0_PAR	DDR	DDR SDRAM0 PAR0
B16	DDR0_ATB1	DDR	DDR0 PHY IO pad Analog Test Bus (ATB)
B17	DDR0_CS_N[2]	DDR	DDR SDRAM0 CS2
B18	DDR0_RESET_N	DDR	DDR SDRAM0 Active Low Asynchronous Reset
B19	DDR0_DQ[14]	DDR	DDR SDRAM0 data [14]
B20	DDR0_DQS_P[1]	DDR	DDR SDRAM0 Data Strobe DQS1_P
B21	VSS	VSS	Digital ground
B22	DDR0_DQ[5]	DDR	DDR SDRAM0 data [5]
B23	DDR0_DQS_P[0]	DDR	DDR SDRAM0 Data Strobe DQS0_P
B25	GPIO[20]	IO	function IO share with GPIO
B26	GPIO[19]	IO	function IO share with GPIO
B27	GPIO[22]	IO	function IO share with GPIO
B28	GPIO[25]	IO	function IO share with GPIO
B29	GPIO[24]	IO	function IO share with GPIO
B30	GPIO[27]	IO	function IO share with GPIO
B31	GPIO[31]	IO	function IO share with GPIO
C1	VSS	VSS	Digital ground
C2	DDR0_DQ[31]	DDR	DDR SDRAM0 data [31]
C3	DDR0_DQS_N[3]	DDR	DDR SDRAM0 Data Strobe DQS3_N
C4	DDR0_DQ[27]	DDR	DDR SDRAM0 data [27]
C6	DDR0_DQ[21]	DDR	DDR SDRAM0 data [21]
C7	DDR0_DQ[18]	DDR	DDR SDRAM0 data [18]
C9	DDR0_ADR[9]	DDR	DDR SDRAM0 Address [9]
C10	DDR0_ADR[0]	DDR	DDR SDRAM0 Address [0]
C12	DDR0_ADR[8]	DDR	DDR SDRAM0 Address [8]
C14	DDR0_BA[0]	DDR	DDR SDRAM0 Bank Address 0
C16	DDR0_ERR_N	DDR	DDR SDRAM0 alert_n
C17	DDR0_CKE[0]	DDR	DDR SDRAM0 Clock0 enable

Pin Number	Pin Name	IO-Type	Description
C19	DDR0_DM_DBI_N[1]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
C20	DDR0_DQ[9]	DDR	DDR SDRAM0 data [9]
C22	DDR0_DQ[4]	DDR	DDR SDRAM0 data [4]
C23	DDR0_DQS_N[0]	DDR	DDR SDRAM0 Data Strobe DQS0_N
C25	GPIO[2]	IO	function IO share with GPIO
C26	GPIO[33]	IO	function IO share with GPIO
C27	GPIO[35]	IO	function IO share with GPIO
C28	GPIO[37]	IO	function IO share with GPIO
C29	GPIO[40]	IO	function IO share with GPIO
C30	GPIO[45]	IO	function IO share with GPIO
C31	GPIO[44]	IO	function IO share with GPIO
D1	FUNC_SHARE[1]	IO	function IO share with group
D2	VSS	VSS	Digital ground
D3	DDR0_DQS_P[3]	DDR	DDR SDRAM0 Data Strobe DQS3_P
D4	DDR0_DM_DBI_N[3]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
D6	DDR0_DM_DBI_N[2]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
D7	DDR0_DQ[17]	DDR	DDR SDRAM0 data [17]
D9	VSS	VSS	Digital ground
D10	DDR0_ADR[3]	DDR	DDR SDRAM0 Address [3]
D12	DDR0_ADR[4]	DDR	DDR SDRAM0 Address [4]
D14	DDR0_RAS_N_ADR16	DDR	DDR SDRAM0 Address 16
D16	DDR0_PLL_REFOUT_N	DDR	DDR0 PHY Differential PLL reference clock output
D17	DDR0_ODT[0]	DDR	DDR SDRAM0 On Die Termination for CS0
D19	DDR0_DQ[13]	DDR	DDR SDRAM0 data [13]
D20	DDR0_DQ[11]	DDR	DDR SDRAM0 data [11]
D22	DDR0_DQ[2]	DDR	DDR SDRAM0 data [2]
D23	VSS	VSS	Digital ground
D25	GPIO[5]	IO	function IO share with GPIO
D26	GPIO[8]	IO	function IO share with GPIO
D27	GPIO[48]	IO	function IO share with GPIO
D28	GPIO[50]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
D29	GPIO[49]	IO	function IO share with GPIO
D30	GPIO[52]	IO	function IO share with GPIO
D31	GPIO[55]	IO	function IO share with GPIO
E1	FUNC_SHARE[0]	IO	function IO share with group
E2	VSS	VSS	Digital ground
E6	DDR0_DQ[22]	DDR	DDR SDRAM0 data [22]
E7	DDR0_DQ[19]	DDR	DDR SDRAM0 data [19]
E9	DDR0_ADR[13]	DDR	DDR SDRAM0 Address [13]
E10	DDR0_ADR[5]	DDR	DDR SDRAM0 Address [5]
E12	DDR0_CAL	DDR	DDR0 PHY IO pad calibration resistor connection
E14	DDR0_CS_N[3]	DDR	DDR SDRAM0 CS3
E16	DDR0_PLL_REFOUT_P	DDR	DDR0 PHY Differential PLL reference clock output
E17	VSS	VSS	Digital ground
E19	DDR0_DQ[12]	DDR	DDR SDRAM0 data [12]
E20	DDR0_DQ[10]	DDR	DDR SDRAM0 data [10]
E22	DDR0_DM_DBI_N[0]	DDR	DDR SDRAM0 Input Data Mask and Data Bus Inversion for byte0
E23	DDR0_DQ[1]	DDR	DDR SDRAM0 data [1]
E25	GPIO[10]	IO	function IO share with GPIO
E26	GPIO[14]	IO	function IO share with GPIO
E27	GPIO[21]	IO	function IO share with GPIO
E28	GPIO[23]	IO	function IO share with GPIO
E29	GPIO[54]	IO	function IO share with GPIO
E30	GPIO[57]	IO	function IO share with GPIO
E31	GPIO[60]	IO	function IO share with GPIO
F1	FUNC_SHARE[6]	IO	function IO share with group
F2	FUNC_SHARE[2]	IO	function IO share with group
F4	FUNC_SHARE[17]	IO	function IO share with group
F5	FUNC_SHARE[12]	IO	function IO share with group
F6	FUNC_SHARE[5]	IO	function IO share with group
F7	VSS	VSS	Digital ground
F9	DDR0_BG[1]	DDR	DDR SDRAM0 Bank Group1
F10	DDR0_ADR[7]	DDR	DDR SDRAM0 Address [7]
F12	DDR0_BA[1]	DDR	DDR SDRAM0 Bank Address 1

Pin Number	Pin Name	IO-Type	Description
F14	DDR0_CAS_N_ADR15	DDR	DDR SDRAM0 Address 15
F16	VSS	VSS	Digital ground
F17	DDR0_CKE[1]	DDR	DDR SDRAM0 Clock1 enable
F19	DDR0_CS_N[0]	DDR	DDR SDRAM0 CS0
F20	VSS	VSS	Digital ground
F22	DDR0_DQ[3]	DDR	DDR SDRAM0 data [3]
F23	DDR0_DQ[0]	DDR	DDR SDRAM0 data [0]
F24	VSS	VSS	Digital ground
F25	GPIO[11]	IO	function IO share with GPIO
F26	GPIO[18]	IO	function IO share with GPIO
F27	GPIO[16]	IO	function IO share with GPIO
F28	GPIO[26]	IO	function IO share with GPIO
F29	GPIO[59]	IO	function IO share with GPIO
F30	GPIO[62]	IO	function IO share with GPIO
F31	GPIO[61]	IO	function IO share with GPIO
G1	FUNC_SHARE[7]	IO	function IO share with group
G2	FUNC_SHARE[3]	IO	function IO share with group
G3	VSS	VSS	Digital ground
G4	FUNC_SHARE[20]	IO	function IO share with group
G5	FUNC_SHARE[9]	IO	function IO share with group
G6	FUNC_SHARE[4]	IO	function IO share with group
G7	VDDQ_DDR0	DDR	DDR IO power
G8	VDDQ_DDR0	DDR	DDR IO power
G9	VDDQ_DDR0	DDR	DDR IO power
G10	VDDQ_DDR0	DDR	DDR IO power
G11	VDDQ_DDR0	DDR	DDR IO power
G12	DDR0_BG[0]	DDR	DDR SDRAM0 Bank Group0
G13	VSS	VSS	Digital ground
G14	DDR0_WE_N_ADR14	DDR	DDR SDRAM0 Address 14
G16	VSS	VSS	Digital ground
G17	DDR0_ODT[1]	DDR	DDR SDRAM0 On Die Termination for CS1
G19	DDR0_PLL_TESTOUT_P	DDR	DDR0 PHY Differential PLL test clock output
G20	VSS	VSS	Digital ground
G22	VSS	VSS	Digital ground

Pin Number	Pin Name	IO-Type	Description
G23	GPIO[4]	IO	function IO share with GPIO
G30	CDTX_L0N	MIPI	MIPI TX Lane-0 with the negative terminal
G31	CDTX_L0P	MIPI	MIPI TX Lane-0 with the positive terminal
H1	FUNC_SHARE[11]	IO	function IO share with group
H2	FUNC_SHARE[10]	IO	function IO share with group
H4	FUNC_SHARE[25]	IO	function IO share with group
H7	VSS	VSS	Digital ground
H8	VDDQ_DDR0	DDR	MIPI TX Lane-3 with the negative terminal
H9	VSS	VSS	Digital ground
H10	VSS	VSS	Digital ground
H11	VDDQ_DDR0	DDR	MIPI TX Lane-4 with the positive terminal
H12	VDDQ_DDR0	DDR	DDR IO power
H13	VDDQ_DDR0	DDR	DDR IO power
H14	VDDQ_DDR0	DDR	DDR IO power
H15	VDDQ_DDR0	DDR	DDR IO power
H16	VSS	VSS	Digital ground
H17	VSS	VSS	Digital ground
H18	VSS	VSS	Digital ground
H19	DDR0_PLL_TESTOUT_N	DDR	DDR0 PHY Differential PLL test clock output
H20	VSS	VSS	Digital ground
H22	GPIO[1]	IO	function IO share with GPIO
H23	GPIO[7]	IO	function IO share with GPIO
H24	GPIO[13]	IO	function IO share with GPIO
H25	GPIO[28]	IO	function IO share with GPIO
H26	GPIO[29]	IO	function IO share with GPIO
H27	GPIO[30]	IO	function IO share with GPIO
H28	GPIO[32]	IO	function IO share with GPIO
H29	GPIO[36]	IO	function IO share with GPIO
H30	CDTX_L1N	MIPI	MIPI TX Lane-1 with the negative terminal
H31	CDTX_L1P	MIPI	MIPI TX Lane-1 with the positive terminal
J1	FUNC_SHARE[22]	IO	function IO share with group
J2	FUNC_SHARE[18]	IO	function IO share with group
J3	FUNC_SHARE[15]	IO	function IO share with group
J4	FUNC_SHARE[14]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
J5	FUNC_SHARE[24]	IO	function IO share with group
J6	FUNC_SHARE[16]	IO	function IO share with group
J7	FUNC_SHARE[8]	IO	function IO share with group
J9	VSS	VSS	Digital ground
J10	VSS	VSS	Digital ground
J11	VDDQ_DDR0	DDR	DDR IO power
J12	VSS	VSS	Digital ground
J13	VDDQ_DDR0	DDR	DDR IO power
J14	VDDQ_DDR0	DDR	DDR IO power
J15	VDDQ_DDR0	DDR	DDR IO power
J16	VSS	VSS	Digital ground
J17	VSS	VSS	Digital ground
J18	VDDQ_DDR0	DDR	DDR IO power
J19	VDDQ_DDR0	DDR	DDR IO power
J20	VDDQ_DDR0	DDR	DDR IO power
J22	VSS	VSS	Digital ground
J23	VSS	VSS	Digital ground
J25	GPIO[34]	IO	function IO share with GPIO
J26	GPIO[38]	IO	function IO share with GPIO
J27	GPIO[41]	IO	function IO share with GPIO
J28	GPIO[39]	IO	function IO share with GPIO
J29	GPIO[42]	IO	function IO share with GPIO
J30	CDTX_L2N	MIPI	MIPI TX Lane-2 with the negative terminal
J31	CDTX_L2P	MIPI	MIPI TX Lane-2 with the positive terminal
K1	FUNC_SHARE[27]	IO	function IO share with group
K2	FUNC_SHARE[23]	IO	function IO share with group
K3	VSS	VSS	Digital ground
K4	FUNC_SHARE[19]	IO	function IO share with group
K5	VSS	VSS	Digital ground
K6	FUNC_SHARE[21]	IO	function IO share with group
K7	FUNC_SHARE[13]	IO	function IO share with group
K8	VSS	VSS	Digital ground
K9	VSS	VSS	Digital ground
K10	VSS	VSS	Digital ground

Pin Number	Pin Name	IO-Type	Description
K11	VSS	VSS	Digital ground
K12	VDDQ_DDR0	DDR	DDR IO power
K13	VDDQ_DDR0	DDR	DDR IO power
K14	VDDQ_DDR0	DDR	DDR IO power
K15	VDDQ_DDR0	DDR	DDR IO power
K16	VDDQ_DDR0	DDR	DDR IO power
K17	VDDQ_DDR0	DDR	DDR IO power
K18	VDDQ_DDR0	DDR	DDR IO power
K19	VDDQ_DDR0	DDR	DDR IO power
K22	VSS	VSS	Digital ground
K23	VSS	VSS	Digital ground
K25	VSS	VSS	Digital ground
K30	CDTX_L3N	MIPI	MIPI TX Lane-3 with the negative terminal
K31	CDTX_L3P	MIPI	MIPI TX Lane-3 with the positive terminal
L1	FUNC_SHARE[26]	IO	function IO share with group
L8	VSS	VSS	Digital ground
L9	VSS	VSS	Digital ground
L10	VSS	VSS	Digital ground
L11	VSS	VSS	Digital ground
L12	VSS	VSS	Digital ground
L13	VSS	VSS	Digital ground
L14	VDDQ_DDR0	DDR	DDR IO power
L15	VDDQCK_DDR0	DDR	DDR CK power
L16	VSS	VSS	Digital ground
L17	VDDPLL_DDR0	DDR	DDR PLL power
L18	VSS	VSS	Digital ground
L19	VSS	VSS	Digital ground
L20	VSS	VSS	Digital ground
L21	VDD	VDD	digital core power
L22	VSS	VSS	Digital ground
L23	VSS	VSS	Digital ground
L25	GPIO[43]	IO	function IO share with GPIO
L26	GPIO[46]	IO	function IO share with GPIO
L27	GPIO[47]	IO	function IO share with GPIO

Pin Number	Pin Name	IO-Type	Description
L28	GPIO[51]	IO	function IO share with GPIO
L29	EXT_RSTN	IO	chip reset, low active
L30	CDTX_L4N	MIPI	MIPI TX Lane-4 with the negative terminal
L31	CDTX_L4P	MIPI	MIPI TX Lane-4 with the positive terminal
M1	FUNC_SHARE[35]	IO	function IO share with group
M2	FUNC_SHARE[34]	IO	function IO share with group
M3	FUNC_SHARE[31]	IO	function IO share with group
M4	FUNC_SHARE[30]	IO	function IO share with group
M5	FUNC_SHARE[32]	IO	function IO share with group
M6	FUNC_SHARE[28]	IO	function IO share with group
M7	FUNC_SHARE[29]	IO	function IO share with group
M8	VDD18	VDDIO	digital IO power
M9	VDD18	VDDIO	digital IO power
M10	VSS	VSS	Digital ground
M11	VSS	VSS	Digital ground
M12	VSS	VSS	Digital ground
M13	VSS	VSS	Digital ground
M14	VSS	VSS	Digital ground
M15	VSS	VSS	Digital ground
M16	VSS	VSS	Digital ground
M17	VSS	VSS	Digital ground
M18	VSS	VSS	Digital ground
M19	VDD	VDD	digital core power
M20	VSS	VSS	Digital ground
M21	VDD	VDD	digital core power
M22	VSS	VSS	Digital ground
M23	AVDD18_MIPITX	AVDD18	MIPI TX analog power
M24	VSS	VSS	Digital ground
M25	GPIO[53]	IO	function IO share with GPIO
M26	GPIO[56]	IO	function IO share with GPIO
M27	GPIO[58]	IO	function IO share with GPIO
M28	GPIO[63]	IO	function IO share with GPIO
M29	TEST_MODE	IO	test mode enable for DFT, high active
M30	CSI2RX_DN5	MIPI	MIPI CSI RX Lane-5 with the negative terminal

Pin Number	Pin Name	IO-Type	Description
M31	CSI2RX_DP5	MIPI	MIPI CSI RX Lane-5 with the positive terminal
N1	FUNC_SHARE[43]	IO	function IO share with group
N2	FUNC_SHARE[38]	IO	function IO share with group
N3	VSS	VSS	Digital ground
N4	FUNC_SHARE[39]	IO	function IO share with group
N5	FUNC_SHARE[37]	IO	function IO share with group
N6	FUNC_SHARE[36]	IO	function IO share with group
N7	FUNC_SHARE[33]	IO	function IO share with group
N8	VDD18	VDDIO	digital IO power
N9	VDD18	VDDIO	digital IO power
N10	VDD18	VDDIO	digital IO power
N11	VDD18	VDDIO	digital IO power
N12	VSS	VSS	Digital ground
N13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
N14	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
N15	VSS	VSS	Digital ground
N16	VSS	VSS	Digital ground
N17	VSS	VSS	Digital ground
N18	VSS	VSS	Digital ground
N19	VDD	VDD	digital core power
N20	VSS	VSS	Digital ground
N21	VDD	VDD	digital core power
N22	VSS	VSS	Digital ground
N24	AVSS_MIPIRX	AVSS	MIPI RX analog ground
N25	VSS	VSS	Digital ground
N30	CSI2RX_DN4	MIPI	MIPI CSI RX Lane-4 with the negative terminal
N31	CSI2RX_DP4	MIPI	MIPI CSI RX Lane-4 with the positive terminal
P1	FUNC_SHARE[42]	IO	function IO share with group
P8	VDD18	VDDIO	digital IO power
P9	VDD18	VDDIO	digital IO power
P10	VDD18	VDDIO	digital IO power
P11	VDD18	VDDIO	digital IO power
P12	VSS	VSS	Digital ground
P13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power

Pin Number	Pin Name	IO-Type	Description
P14	VSS	VSS	Digital ground
P15	VSS	VSS	Digital ground
P16	VDD	VDD	digital core power
P17	VDD	VDD	digital core power
P18	VSS	VSS	Digital ground
P19	VDD	VDD	digital core power
P20	VSS	VSS	Digital ground
P21	VDD	VDD	digital core power
P22	VSS	VSS	Digital ground
P23	AVDD09_MIPIRX	AVDD	MIPI RX analog power
P24	VSS	VSS	Digital ground
P25	QSPI_DATA[3]	IO	QSPI serial data [3]
P26	QSPI_DATA[2]	IO	QSPI serial data [2]
P27	QSPI_CSN0	IO	SPI Flash chip select 0, low active
P28	FUNC_SHARE[130]	IO	function IO share with group
P29	FUNC_SHARE[136]	IO	function IO share with group
P30	CSI2RX_DN3	MIPI	MIPI CSI RX Lane-3 with the negative terminal
P31	CSI2RX_DP3	MIPI	MIPI CSI RX Lane-3 with the positive terminal
R1	FUNC_SHARE[50]	IO	function IO share with group
R2	FUNC_SHARE[47]	IO	function IO share with group
R3	FUNC_SHARE[46]	IO	function IO share with group
R4	FUNC_SHARE[45]	IO	function IO share with group
R5	FUNC_SHARE[44]	IO	function IO share with group
R6	FUNC_SHARE[41]	IO	function IO share with group
R7	FUNC_SHARE[40]	IO	function IO share with group
R8	VDD18	VDDIO	digital IO power
R9	VDD18	VDDIO	digital IO power
R10	VDD18	VDDIO	digital IO power
R11	VDD18	VDDIO	digital IO power
R12	VSS	VSS	Digital ground
R13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
R14	VSS	VSS	Digital ground
R15	VSS	VSS	Digital ground
R16	VDD	VDD	digital core power

Pin Number	Pin Name	IO-Type	Description
R17	VDD	VDD	digital core power
R18	VDD	VDD	digital core power
R19	VDD	VDD	digital core power
R20	VSS	VSS	Digital ground
R21	VDD	VDD	digital core power
R22	VSS	VSS	Digital ground
R23	VSS	VSS	Digital ground
R25	QSPI_CLK	IO	SPI NAND/NOR Flash device clock
R26	QSPI_DATA[0]	IO	QSPI serial data [0]
R27	QSPI_DATA[1]	IO	QSPI serial data [1]
R28	FUNC_SHARE[140]	IO	function IO share with group
R29	FUNC_SHARE[118]	IO	function IO share with group
R30	CSI2RX_DN2	MIPI	MIPI CSI RX Lane-2 with the negative terminal
R31	CSI2RX_DP2	MIPI	MIPI CSI RX Lane-2 with the positive terminal
T1	FUNC_SHARE[51]	IO	function IO share with group
T2	FUNC_SHARE[52]	IO	function IO share with group
T3	VSS	VSS	Digital ground
T4	FUNC_SHARE[55]	IO	function IO share with group
T5	FUNC_SHARE[53]	IO	function IO share with group
T6	FUNC_SHARE[49]	IO	function IO share with group
T7	FUNC_SHARE[48]	IO	function IO share with group
T9	VSS	VSS	Digital ground
T10	VSS	VSS	Digital ground
T11	VSS	VSS	Digital ground
T12	VSS	VSS	Digital ground
T13	VDD3318_CHIPLINK	VDD3318	FUNC_SHARE[0-69] IO power
T14	VSS	VSS	Digital ground
T15	VDD	VDD	digital core power
T16	VDD	VDD	digital core power
T17	VDD	VDD	digital core power
T18	VDD	VDD	digital core power
T19	VDD	VDD	digital core power
T20	VDD	VDD	digital core power
T21	VDD	VDD	digital core power

Pin Number	Pin Name	IO-Type	Description
T22	VSS	VSS	Digital ground
T23	AVDD18_MIPIRX	AVDD18	MIPI RX analog power supply for LDO
T24	VSS	VSS	Digital ground
T25	VSS	VSS	Digital ground
T30	CSI2RX_DN1	MIPI	MIPI CSI RX Lane-1 with the negative terminal
T31	CSI2RX_DP1	MIPI	MIPI CSI RX Lane-1 with the positive terminal
U1	FUNC_SHARE[54]	IO	function IO share with group
U8	VSS	VSS	Digital ground
U9	VSS	VSS	Digital ground
U10	VSS	VSS	Digital ground
U11	VSS	VSS	Digital ground
U12	VSS	VSS	Digital ground
U13	VSS	VSS	Digital ground
U14	VDD	VDD	digital core power
U15	VDD	VDD	digital core power
U16	VDD	VDD	digital core power
U17	VDD	VDD	digital core power
U18	VSS	VSS	Digital ground
U19	VSS	VSS	Digital ground
U20	AVSS_PLL0	AVSS	PLL0 analog ground
U21	AVDD09_PLL0	AVDD	PLL0 analog power
U22	AVDD09_PLL1	AVDD	PLL1 analog power
U23	AVSS_PLL1	AVSS	PLL1 analog ground
U24	ANA18_TEMP_TEST1	AIO	Analog test access
U25	ANA18_TEMP_TEST0	AIO	Analog test access
U26	FUNC_SHARE[137]	IO	function IO share with group
U27	FUNC_SHARE[138]	IO	function IO share with group
U28	FUNC_SHARE[132]	IO	function IO share with group
U29	FUNC_SHARE[116]	IO	function IO share with group
U30	CSI2RX_DN0	MIPI	MIPI CSI RX Lane-0 with the negative terminal
U31	CSI2RX_DP0	MIPI	MIPI CSI RX Lane-0 with the positive terminal
V1	FUNC_SHARE[56]	IO	function IO share with group
V2	FUNC_SHARE[57]	IO	function IO share with group
V3	FUNC_SHARE[60]	IO	function IO share with group

Pin Number	Pin Name	IO-Type	Description
V4	FUNC_SHARE[61]	IO	function IO share with group
V5	FUNC_SHARE[59]	IO	function IO share with group
V6	FUNC_SHARE[58]	IO	function IO share with group
V7	FUNC_SHARE[63]	IO	function IO share with group
V8	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
V9	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
V10	VSS	VSS	Digital ground
V11	VSS	VSS	Digital ground
V12	VSS	VSS	Digital ground
V13	VSS	VSS	Digital ground
V14	VDD	VDD	digital core power
V15	VDD	VDD	digital core power
V16	VDD	VDD	digital core power
V17	VDD	VDD	digital core power
V18	VSS	VSS	Digital ground
V19	VSS	VSS	Digital ground
V20	AVSS_PLL2	AVSS	PLL2 analog ground
V21	AVDD09_PLL2	AVDD	PLL2 analog power
V24	ANA18_TEMP_VSS	AIO	Ground sense, VSS return output
V25	ANA18_TEMP_VCAL	AIO	Calibration voltage input,700mV±20mV
V26	FUNC_SHARE[133]	IO	function IO share with group
V27	FUNC_SHARE[127]	IO	function IO share with group
V28	FUNC_SHARE[131]	IO	function IO share with group
V29	FUNC_SHARE[122]	IO	function IO share with group
V30	OSC1_XIN	OSC	27MHz crystal input
V31	OSC1_XOUT	OSC	27MHz crystal output
W1	FUNC_SHARE[64]	IO	function IO share with group
W2	FUNC_SHARE[65]	IO	function IO share with group
W3	VSS	VSS	Digital ground
W4	FUNC_SHARE[68]	IO	function IO share with group
W5	FUNC_SHARE[62]	IO	function IO share with group
W6	FUNC_SHARE[67]	IO	function IO share with group
W7	FUNC_SHARE[66]	IO	function IO share with group
W8	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power

Pin Number	Pin Name	IO-Type	Description
W9	VDD3318_LCD	VDD3318	FUNC_SHARE[70-97] IO power
W10	VSS	VSS	Digital ground
W11	VDD	VDD	digital core power
W12	VSS	VSS	Digital ground
W13	VSS	VSS	Digital ground
W14	VDD	VDD	digital core power
W15	VDD	VDD	digital core power
W16	VDD	VDD	digital core power
W17	VDD	VDD	digital core power
W18	VDD	VDD	digital core power
W19	VDD	VDD	digital core power
W20	VSS	VSS	Digital ground
W21	VSS	VSS	Digital ground
W23	AVDD18_TS	AVDD18	Temperature sensor analog power
W24	VSS18_TS	VSS	Temperature sensor analog ground
W25	VSS	VSS	Digital ground
W27	FUNC_SHARE[126]	IO	function IO share with group
W28	FUNC_SHARE[123]	IO	function IO share with group
W30	VSS	VSS	Digital ground
W31	VSS	VSS	Digital ground
Y1	FUNC_SHARE[69]	IO	function IO share with group
Y2	FUNC_SHARE[73]	IO	function IO share with group
Y8	VSS	VSS	Digital ground
Y9	VSS	VSS	Digital ground
Y10	VSS	VSS	Digital ground
Y11	VDD	VDD	digital core power
Y12	VDD	VDD	digital core power
Y13	VDD	VDD	digital core power
Y14	VSS	VSS	Digital ground
Y15	VDD	VDD	digital core power
Y16	VSS	VSS	Digital ground
Y17	VSS	VSS	Digital ground
Y18	VSS	VSS	Digital ground
Y19	VSS	VSS	Digital ground

Pin Number	Pin Name	IO-Type	Description
Y20	VSS	VSS	Digital ground
Y21	VDD3318_GMII	VDD3318	FUNC_SHARE[115-141] IO power
Y25	FUNC_SHARE[129]	IO	function IO share with group
Y26	FUNC_SHARE[134]	IO	function IO share with group
Y27	FUNC_SHARE[135]	IO	function IO share with group
Y28	FUNC_SHARE[139]	IO	function IO share with group
Y29	FUNC_SHARE[141]	IO	function IO share with group
Y30	OSC0_XIN	OSC	25MHz crystal input
Y31	OSC0_XOUT	OSC	25MHz crystal output

10.2. Package Ball Map

Table 10-2 Package Ball Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
A	DDR0_DQ[30]	DDR0_DQ[24]	DDR0_DQ[26]	VSS	DDR0_DQ[16]	DDR0_DQS_P[2]	VSS		DDR0_ACT_N	DDR0_ADR[11]	VSS	DDR0_CK_P[1]		DDR0_CK_P[0]	DDR0_ADR[2]	DDR0_ATB0	DDR0_CS_N[1]	VSS	DDR0_DQ[15]	DDR0_DQS_N[1]	DDR0_DQ[8]	DDR0_DQ[7]	DDR0_DQ[6]		GPIO[0]	GPIO[3]	GPIO[6]	GPIO[9]	GPIO[12]	GPIO[15]	GPIO[17]
B	DDR0_DQ[29]	DDR0_DQ[28]	DDR0_DQ[25]	DDR0_DQ[23]	DDR0_DQ[20]	DDR0_DQS_N[2]	DDR0_ADR[12]		DDR0_ADR[6]	DDR0_ADR[1]	DDR0_ADR[10]	DDR0_CK_N[1]		DDR0_CK_N[0]	DDR0_PAR	DDR0_ATB1	DDR0_CS_N[2]	DDR0_RESETN	DDR0_DQ[14]	DDR0_DQS_P[1]	VSS	DDR0_DQ[5]	DDR0_DQS_P[0]		GPIO[20]	GPIO[19]	GPIO[22]	GPIO[25]	GPIO[24]	GPIO[27]	GPIO[31]
C	VSS	DDR0_DQ[31]	DDR0_DQS_N[3]	DDR0_DQ[27]		DDR0_DQ[21]	DDR0_DQ[18]		DDR0_ADR[9]	DDR0_ADR[0]		DDR0_ADR[8]		DDR0_BA[0]		DDR0_ERR_N	DDR0_CKE[0]		DDR0_DM_DBI_N[1]	DDR0_DQ[9]		DDR0_DQ[4]	DDR0_DQS_N[0]		GPIO[2]	GPIO[33]	GPIO[35]	GPIO[37]	GPIO[40]	GPIO[45]	GPIO[44]
D	FUNC_SHARE[1]	VSS	DDR0_DQS_P[3]	DDR0_DM_DBI_N[3]		DDR0_DM_DBI_N[2]	DDR0_DQ[17]		VSS	DDR0_ADR[3]		DDR0_ADR[4]		DDR0_RAS_N_ADR16		DDR0_PLL_REFOUT_N	DDR0_ODT[0]		DDR0_DQ[13]	DDR0_DQ[11]		DDR0_DQ[2]	VSS		GPIO[5]	GPIO[8]	GPIO[48]	GPIO[50]	GPIO[49]	GPIO[52]	GPIO[55]
E	FUNC_SHARE[0]	VSS				DDR0_DQ[22]	DDR0_DQ[19]		DDR0_ADR[13]	DDR0_ADR[5]		DDR0_CAL		DDR0_CS_N[3]		DDR0_PLL_REFOUT_P	VSS		DDR0_DQ[12]	DDR0_DQ[10]		DDR0_DM_DBI_N[0]	DDR0_DQ[1]		GPIO[10]	GPIO[14]	GPIO[21]	GPIO[23]	GPIO[54]	GPIO[57]	GPIO[60]
F	FUNC_SHARE[6]	FUNC_SHARE[2]		FUNC_SHARE[17]	FUNC_SHARE[12]	FUNC_SHARE[5]	VSS		DDR0_BG[1]	DDR0_ADR[7]		DDR0_BA[1]		DDR0_CAS_N_ADR15		VSS	DDR0_CKE[1]		DDR0_CS_N[0]	VSS		DDR0_DQ[3]	DDR0_DQ[0]	VSS	GPIO[11]	GPIO[18]	GPIO[16]	GPIO[26]	GPIO[59]	GPIO[62]	GPIO[61]
G	FUNC_SHARE[7]	FUNC_SHARE[3]	VSS	FUNC_SHARE[20]	FUNC_SHARE[9]	FUNC_SHARE[4]	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	DDR0_BG[0]	VSS	DDR0_WE_N_ADR14		VSS	DDR0_ODT[1]		DDR0_PLL_TESTOUT_P	VSS		VSS	GPIO[4]							CDTX_L0N	CDTX_L0P
H	FUNC_SHARE[11]	FUNC_SHARE[10]		FUNC_SHARE[25]			VSS	VDDQ_DDR0	VSS	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VSS	VSS	VSS	DDR0_PLL_TESTOUT_N	VSS		GPIO[1]	GPIO[7]	GPIO[13]	GPIO[28]	GPIO[29]	GPIO[30]	GPIO[32]	GPIO[36]	CDTX_L1N	CDTX_L1P
J	FUNC_SHARE[22]	FUNC_SHARE[18]	FUNC_SHARE[15]	FUNC_SHARE[14]	FUNC_SHARE[24]	FUNC_SHARE[16]	FUNC_SHARE[8]		VSS	VSS	VDDQ_DDR0	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VSS	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0		VSS	VSS		GPIO[34]	GPIO[38]	GPIO[41]	GPIO[39]	GPIO[42]	CDTX_L2N	CDTX_L2P
K	FUNC_SHARE[27]	FUNC_SHARE[23]	VSS	FUNC_SHARE[19]	VSS	FUNC_SHARE[21]	FUNC_SHARE[13]	VSS	VSS	VSS	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0	VDDQ_DDR0			VSS	VSS		VSS					CDTX_L3N	CDTX_L3P
L	FUNC_SHARE[26]							VSS	VSS	VSS	VSS	VSS	VSS	VDDQ_DDR0	VDDQCK_DDR0	VSS	VDDPLL_DDR0	VSS	VSS	VSS	VDD	VSS	VSS		GPIO[43]	GPIO[46]	GPIO[47]	GPIO[51]	EXT_RSTN	CDTX_L4N	CDTX_L4P
M	FUNC_SHARE[35]	FUNC_SHARE[34]	FUNC_SHARE[31]	FUNC_SHARE[30]	FUNC_SHARE[32]	FUNC_SHARE[28]	FUNC_SHARE[29]	VDD18	VDD18	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDD	VSS	VDD	VSS	AVDD18_MIPITX	VSS	GPIO[53]	GPIO[56]	GPIO[58]	GPIO[63]	TEST_MODE	CSI2RX_DN5	CSI2RX_DP5
N	FUNC_SHARE[43]	FUNC_SHARE[38]	VSS	FUNC_SHARE[39]	FUNC_SHARE[37]	FUNC_SHARE[36]	FUNC_SHARE[33]	VDD18	VDD18	VDD18	VDD18	VSS	VDD3318_CHIPLINK	VDD3318_CHIPLINK	VSS	VSS	VSS	VSS	VDD	VSS	VDD	VSS		AVSS_MIPIRX	VSS					CSI2RX_DN4	CSI2RX_DP4
P	FUNC_SHARE[42]							VDD18	VDD18	VDD18	VDD18	VSS	VDD3318_CHIPLINK	VSS	VSS	VDD	VDD	VSS	VDD	VSS	VDD	VSS	AVDD09_MIPIRX	VSS	QSPI_DATA[3]	QSPI_DATA[2]	QSPI_CSN0	FUNC_SHARE[130]	FUNC_SHARE[136]	CSI2RX_DN3	CSI2RX_DP3
R	FUNC_SHARE[50]	FUNC_SHARE[47]	FUNC_SHARE[46]	FUNC_SHARE[45]	FUNC_SHARE[44]	FUNC_SHARE[41]	FUNC_SHARE[40]	VDD18	VDD18	VDD18	VDD18	VSS	VDD3318_CHIPLINK	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VDD	VSS	VSS		QSPI_CLK	QSPI_DATA[0]	QSPI_DATA[1]	FUNC_SHARE[140]	FUNC_SHARE[118]	CSI2RX_DN2	CSI2RX_DP2
T	FUNC_SHARE[51]	FUNC_SHARE[52]	VSS	FUNC_SHARE[55]	FUNC_SHARE[53]	FUNC_SHARE[49]	FUNC_SHARE[48]		VSS	VSS	VSS	VSS	VDD3318_CHIPLINK	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VDD	VSS	AVDD18_MIPIRX	VSS	VSS					CSI2RX_DN1	CSI2RX_DP1
U	FUNC_SHARE[54]							VSS	VSS	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	AVSS_PLL0	AVDD09_PLL0	AVDD09_PLL1	AVSS_PLL1	ANA18_TEMP_TEST1	ANA18_TEMP_TEST0	FUNC_SHARE[137]	FUNC_SHARE[138]	FUNC_SHARE[132]	FUNC_SHARE[116]	CSI2RX_DN0	CSI2RX_DP0
V	FUNC_SHARE[56]	FUNC_SHARE[57]	FUNC_SHARE[60]	FUNC_SHARE[61]	FUNC_SHARE[59]	FUNC_SHARE[58]	FUNC_SHARE[63]	VDD3318_LCD	VDD3318_LCD	VSS	VSS	VSS	VSS	VDD	VDD	VDD	VDD	VSS	VSS	AVSS_PLL2	AVDD09_PLL2			ANA18_TEMP_VSS	ANA18_TEMP_VCAL	FUNC_SHARE[133]	FUNC_SHARE[127]	FUNC_SHARE[131]	FUNC_SHARE[122]	OSC1_XIN	OSC1_XOUT
W	FUNC_SHARE[64]	FUNC_SHARE[65]	VSS	FUNC_SHARE[68]	FUNC_SHARE[62]	FUNC_SHARE[67]	FUNC_SHARE[66]	VDD3318_LCD	VDD3318_LCD	VSS	VDD	VSS	VSS	VDD	VDD	VDD	VDD	VDD	VDD	VSS	VSS		AVDD18_TS	VSS18_TS	VSS		FUNC_SHARE[126]	FUNC_SHARE[123]		VSS	VSS
Y	FUNC_SHARE[69]	FUNC_SHARE[73]						VSS	VSS	VSS	VDD	VDD	VDD	VSS	VDD	VSS	VSS	VSS	VSS	VSS	VDD3318_GMII				FUNC_SHARE[129]	FUNC_SHARE[134]	FUNC_SHARE[135]	FUNC_SHARE[139]	FUNC_SHARE[141]	OSC0_XIN	OSC0_XOUT
AA	FUNC_SHARE[72]	FUNC_SHARE[77]	FUNC_SHARE[70]	FUNC_SHARE[71]	FUNC_SHARE[74]	FUNC_SHARE[75]		VSS	VDD3318_SENSOR	VSS	VDD	VSS	VSS	VSS	VSS	VDDQCK_DDR1	VSS	VDDPLL_DDR1	VSS	VSS	VDD3318_GMII	VSS	AVDD33_USB	AVSS_USB	FUNC_SHARE[121]	FUNC_SHARE[120]	FUNC_SHARE[115]	FUNC_SHARE[124]	VSS	FUNC_SHARE[125]	FUNC_SHARE[128]
AB	FUNC_SHARE[76]	FUNC_SHARE[81]	VSS	FUNC_SHARE[85]	FUNC_SHARE[78]	FUNC_SHARE[79]	FUNC_SHARE[82]	VSS	VDD3318_SENSOR	VSS	VSS	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VDDQ_DDR1	VSS	VSS	DVDD18_OTP	VSS18_OTP									FUNC_SHARE[117]	FUNC_SHARE[119]
AC	FUNC_SHARE[80]							VSS	VSS	VSS	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VSS	VDDQ_DDR1	VSS	VDDQ_DDR1	VSS	VSS	ANA18_OTP_PENVDD2	VSS	AVDD09TX_USB	AVSSTX_USB	VSS	USB_SSTXB1	USB_SSTXA1	USB_DP	USB_DM	USB_SSRXB2	USB_SSRXA2
AD	FUNC_SHARE[84]	FUNC_SHARE[89]	FUNC_SHARE[92]	FUNC_SHARE[96]	FUNC_SHARE[97]	FUNC_SHARE[102]	FUNC_SHARE[101]	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VSS	VSS	VDDQ_DDR1	VDDQ_DDR1	VDDQ_DDR1	VSS	VSS	VSS	VSS	AVDD09RX_USB	AVDD18_USB	VSS	USB_SSRXB1	USB_SSRXA1	VSS	VSS	USB_SSTXA2	USB_SSTXB2
AE	FUNC_SHARE[88]	FUNC_SHARE[93]	VSS	FUNC_SHARE[94]	FUNC_SHARE[104]	FUNC_SHARE[108]	FUNC_SHARE[112]	VSS	VDDQ_DDR1	VDDQ_DDR1	VSS	VDDQ_DDR1	DDR1_ADR[9]	VSS	VSS	DDR1_BG[0]	VDDQ_DDR1	DDR1_CAS_N_ADR15	VDDQ_DDR1	VSS	VDDQ_DDR1	VDDQ_DDR1	AVSSRX_USB	VSS							VSS
AF	FUNC_SHARE[99]						DDR1_DQ[31]	DDR1_DQ[28]		DDR1_DQ[23]	DDR1_DQ[22]		DDR1_ADR[6]	DDR1_ADR[3]		DDR1_BA[1]		DDR1_WE_N_ADR14		DDR1_CS_N[3]	DDR1_PLL_REFOUT_N		DDR1_DQ[15]	DDR1_DQ[14]		DDR1_DQ[8]	VSS		DDR1_DQ[0]	DDR1_DQ[3]	
AG	FUNC_SHARE[100]	FUNC_SHARE[83]	FUNC_SHARE[87]	FUNC_SHARE[91]	VSS		DDR1_DQ[30]	DDR1_DQ[29]		DDR1_DQ[20]	DDR1_DM_DBI_N[2]			DDR1_ADR[5]		DDR1_ADR[0]		VSS		DDR1_CAL	DDR1_PLL_REFOUT_P		DDR1_CKE[0]	VSS		DDR1_DQ[11]	DDR1_DQ[10]		DDR1_DQ[1]	DDR1_DM_DBI_N[0]	
AH	FUNC_SHARE[103]	FUNC_SHARE[86]	VSS	FUNC_SHARE[95]	FUNC_SHARE[106]		VSS	DDR1_DM_DBI_N[3]		VSS	DDR1_DQ[21]		VSS	DDR1_ADR[7]		VSS		DDR1_PAR		DDR1_CS_N[2]	DDR1_CS_N[1]		DDR1_ODT[1]	DDR1_ODT[0]		VSS	DDR1_DQ[9]		VSS	DDR1_DQ[2]	
AJ	FUNC_SHARE[105]						DDR1_DQS_P[3]	DDR1_DQ[27]		DDR1_DQS_N[2]	DDR1_DQ[19]	DDR1_BG[1]	DDR1_ADR[12]	DDR1_ADR[10]		DDR1_ADR[2]		DDR1_ADR[1]		DDR1_ERR_N	VSS		VSS	DDR1_CKE[1]		DDR1_DM_DBI_N[1]	DDR1_DQS_P[1]		DDR1_DQ[4]	DDR1_DQS_N[0]	
AK	FUNC_SHARE[107]	FUNC_SHARE[109]	VSS	FUNC_SHARE[98]	VSS		DDR1_DQS_N[3]	DDR1_DQ[26]		DDR1_DQS_P[2]	DDR1_DQ[17]	DDR1_ADR[13]	DDR1_ACT_N	DDR1_ADR[8]		DDR1_CK_N[1]		DDR1_CK_N[0]		DDR1_RAS_NADR16	DDR1_ATB0		DDR1_CS_N[0]	DDR1_PLL_TESTOUT_N		VSS	DDR1_DQS_N[1]		DDR1_DQ[5]	DDR1_DQS_P[0]	
AL	FUNC_SHARE[111]	FUNC_SHARE[113]	FUNC_SHARE[90]	FUNC_SHARE[110]	FUNC_SHARE[114]	VSS	DDR1_DQ[25]	DDR1_DQ[24]	VSS	DDR1_DQ[18]	DDR1_DQ[16]	VSS	DDR1_ADR[11]	DDR1_ADR[4]	VSS	DDR1_CK_P[1]		DDR1_CK_P[0]	VSS	DDR1_BA[0]	DDR1_ATB1	VSS	DDR1_RESET_N	DDR1_PLL_TESTOUT_P	VSS	DDR1_DQ[13]	DDR1_DQ[12]	VSS	DDR1_DQ[7]	DDR1_DQ[6]	

11. Function IO Share

The IO_PADSHARE_SEL register can be programmed to select one of the pre-defined multiplexed signal groups on PAD_FUNC_SHARE and PAD_GPIO device pads. In the table below each value in the register selects one of the multiplexed signal groups labelled as **Function 0**, **Function 1**, … **Function 6** (these 7 functions can be thought of as 7 configurations of the device.) So as an example if IO_PADSHARE_SEL is programmed to a 1 then the signals multiplexed on these device pads are listed in the column **Function 1** of the table. As such, with IO_PADSHARE_SEL = 1, the signal LCD_CLK is made available on PAD_FUNC_SHARE[0], the signal LCD_DE is made available on PAD_FUNC_SHARE[1] and so on. Simultaneously PAD_GPIO[0] gets configured as GPIO0, PAD_GPIO[1] gets configured as GPIO1 and so on. On Power-up rest the pads get configured as shown in the Function 0 column (since the IO_PADSHARE_SEL gets set to 0 on Power-up reset.) Note if a cell is left blank in the columns Function 0, … Function 6 then it means that the corresponding device pad is not configured for any internal or external signal, i.e., it is an unused device pad.

Each device pad has four programmable I/O attributes along with a default signal that can be multiplexed onto it. These attributes are:

1. **Input Enable**: When enabled the I/O pad functions as an input.
2. **Output Enable**: When enabled the I/O pad functions as an output.
3. **Pull Up**: When enabled an internal pull up resistor is provided on the I/O pad.
4. **Pull Down**: When enabled an internal pull down resistor is provided on the I/O pad.
5. **Schmitt Trigger**: When enabled a Schmitt trigger function is provided on the I/O pad.

All these attributes can be programmed independently for each device pad and it is the responsibility of the user to use these attributes for a device pad in a logical and coherent manner. A default value exits for all these programmable attributes (with certain exceptions) which are available after Power-up reset resulting in a default configuration for the device pads. These default attributes are listed under the **Default Configuration** column in the table below. If a user wants to use a particular device pad differently than the default configuration (determined by the default attributes) then it is their responsibility to program the attributes appropriately.

On Power-up (after reset) a device pad, by default, gets configured either as an **Input** (Input Enable = *enable*, Output Enable = *disable*) or as an **Output** (Input Enable = *disable*, Output Enable = *enable*). Some device pads do not get configured by default either as input or output (they have both Input Enable = *disable* and Output Enable = *disable*.) These device pads are highlighted in blue color as a reminder to the user to configure these device pads appropriately (depending on how the device pad will being used.)

For some device pads it is not possible to change a particular attribute from its default value. This is specified in the table below, as:

1. **NA** (Not Applicable): meaning that the attribute is just not available for the particular device pad *OR*
2. **Constant enable**: meaning that the attribute cannot be programmed but it is hardwired as an *enable*.

Table 11-1 Function IO Share with Interface Group Description

Interface	IO Name	Function 0 (Default)	Function 1	Function 2	Function 3	Function4	Function5	Function6	Default Configuration				
									Pull Up	Pull Down	Input Enable	Output Enable	Schmitt Trigger
ChipLink	PAD_FUNC_SHARE[0]	X2C_TX_CLK	LCD_CLK	CM_CLK	X2C_TX_CLK	GPIO0	GPIO0	GPIO0	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[1]	X2C_TX_RST	LCD_DE	CM_VSYNC	X2C_TX_RST	GPIO1	GPIO1	GPIO1	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[2]	X2C_TX_SEND	LCD_VSYNC	CM_HSYNC	X2C_TX_SEND	GPIO2	GPIO2	GPIO2	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[3]	X2C_TX_DATA0	LCD_HSYNC	CM_DATA0	X2C_TX_DATA0	GPIO3	GPIO3	GPIO3	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[4]	X2C_TX_DATA1	LCD_DATA0	CM_DATA1	X2C_TX_DATA1	GPIO4	GPIO4	GPIO4	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[5]	X2C_TX_DATA2	LCD_DATA1	CM_DATA2	X2C_TX_DATA2	GPIO5	GPIO5	GPIO5	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[6]	X2C_TX_DATA3	LCD_DATA2	CM_DATA3	X2C_TX_DATA3	GPIO6	GPIO6	GPIO6	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[7]	X2C_TX_DATA4	LCD_DATA3	CM_DATA4	X2C_TX_DATA4	GPIO7	GPIO7	GPIO7	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[8]	X2C_TX_DATA5	LCD_DATA4	CM_DATA5	X2C_TX_DATA5	GPIO8	GPIO8	GPIO8	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[9]	X2C_TX_DATA6	LCD_DATA5	CM_DATA6	X2C_TX_DATA6	GPIO9	GPIO9	GPIO9	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[10]	X2C_TX_DATA7	LCD_DATA6	CM_DATA7	X2C_TX_DATA7	GPIO10	GPIO10	GPIO10	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[11]	X2C_TX_DATA8	LCD_DATA7	CM_DATA8	X2C_TX_DATA8	GPIO11	GPIO11	GPIO11	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[12]	X2C_TX_DATA9	LCD_DATA8	CM_DATA9	X2C_TX_DATA9	GPIO12	GPIO12	GPIO12	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[13]	X2C_TX_DATA10	LCD_DATA9	CM_DATA10	X2C_TX_DATA10	GPIO13	GPIO13	GPIO13	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[14]	X2C_TX_DATA11	LCD_DATA10	CM_DATA11	X2C_TX_DATA11	GPIO14	GPIO14	GPIO14	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[15]	X2C_TX_DATA12	LCD_DATA11	CM_DATA12	X2C_TX_DATA12	GPIO15	GPIO15	GPIO15	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[16]	X2C_TX_DATA13	LCD_DATA12	CM_DATA13	X2C_TX_DATA13	GPIO16	GPIO16	GPIO16	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[17]	X2C_TX_DATA14	LCD_DATA13	GMAC_PHY_GTXCLK	X2C_TX_DATA14	GPIO17	GPIO17	GPIO17	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[18]	X2C_TX_DATA15	LCD_DATA14	GMAC_PHY_MIITXCLK	X2C_TX_DATA15	GPIO18	GPIO18	GPIO18	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[19]	X2C_TX_DATA16	LCD_DATA15	GMAC_PHY_TXEN	X2C_TX_DATA16	GPIO19	GPIO19	GPIO19	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[20]	X2C_TX_DATA17	LCD_DATA16	GMAC_PHY_TXER	X2C_TX_DATA17	GPIO20	GPIO20	GPIO20	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[21]	X2C_TX_DATA18	LCD_DATA17	GMAC_PHY_TXD0	X2C_TX_DATA18	GPIO21	GPIO21	GPIO21	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[22]	X2C_TX_DATA19	LCD_DATA18	GMAC_PHY_TXD1	X2C_TX_DATA19	GPIO22	GPIO22	GPIO22	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[23]	X2C_TX_DATA20	LCD_DATA19	GMAC_PHY_TXD2	X2C_TX_DATA20	GPIO23	GPIO23	GPIO23	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[24]	X2C_TX_DATA21	LCD_DATA20	GMAC_PHY_TXD3	X2C_TX_DATA21	GPIO24	GPIO24	GPIO24	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[25]	X2C_TX_DATA22	LCD_DATA21	GMAC_PHY_TXD4	X2C_TX_DATA22	GPIO25	GPIO25	GPIO25	Disable	Disable	Disable	Enable	Disable

	PAD_FUNC_SHARE[26]	X2C_TX_DATA23	LCD_DATA22	GMAC_PHY_TXD5	X2C_TX_DATA23	GPIO26	GPIO26	GPIO26	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[27]	X2C_TX_DATA24	LCD_DATA23	GMAC_PHY_TXD6	X2C_TX_DATA24	GPIO27	GPIO27	GPIO27	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[28]	X2C_TX_DATA25	CM_CLK	GMAC_PHY_TXD7	X2C_TX_DATA25	GPIO28	GPIO28	GPIO28	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[29]	X2C_TX_DATA26	CM_VSYNC	GMAC_PHY_RXCLK	X2C_TX_DATA26	GPIO29	GPIO29	GPIO29	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[30]	X2C_TX_DATA27	CM_HSYNC	GMAC_PHY_RXDV	X2C_TX_DATA27	GPIO30	GPIO30	GPIO30	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[31]	X2C_TX_DATA28	CM_DATA0	GMAC_PHY_RXER	X2C_TX_DATA28	GPIO31	GPIO31	GPIO31	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[32]	X2C_TX_DATA29	CM_DATA1	GMAC_PHY_RXD0	X2C_TX_DATA29	GPIO32	GPIO32	GPIO32	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[33]	X2C_TX_DATA30	CM_DATA2	GMAC_PHY_RXD1	X2C_TX_DATA30	GPIO33	GPIO33	GPIO33	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[34]	X2C_TX_DATA31	CM_DATA3	GMAC_PHY_RXD2	X2C_TX_DATA31	GPIO34	GPIO34	GPIO34	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[35]	X2C_RX_CLK	CM_DATA4	GMAC_PHY_RXD3	X2C_RX_CLK	GPIO35	GPIO35	GPIO35	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[36]	X2C_RX_RST	CM_DATA5	GMAC_PHY_RXD4	X2C_RX_RST	GPIO36	GPIO36	GPIO36	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[37]	X2C_RX_SEND	CM_DATA6	GMAC_PHY_RXD5	X2C_RX_SEND	GPIO37	GPIO37	GPIO37	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[38]	X2C_RX_DATA0	CM_DATA7	GMAC_PHY_RXD6	X2C_RX_DATA0	GPIO38	GPIO38	GPIO38	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[39]	X2C_RX_DATA1	CM_DATA8	GMAC_PHY_RXD7	X2C_RX_DATA1	GPIO39	GPIO39	GPIO39	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[40]	X2C_RX_DATA2	CM_DATA9	GMAC_PHY_CRS	X2C_RX_DATA2	GPIO40	GPIO40	GPIO40	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[41]	X2C_RX_DATA3	CM_DATA10	GMAC_PHY_COL	X2C_RX_DATA3	GPIO41	GPIO41	GPIO41	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[42]	X2C_RX_DATA4	CM_DATA11	GMAC_MDC	X2C_RX_DATA4	GPIO42	GPIO42	GPIO42	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[43]	X2C_RX_DATA5	CM_DATA12	GMAC_MDIO	X2C_RX_DATA5	GPIO43	GPIO43	GPIO43	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[44]	X2C_RX_DATA6	CM_DATA13	LCD_CLK	X2C_RX_DATA6	GPIO44	GPIO44	GPIO44	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[45]	X2C_RX_DATA7	GMAC_PHY_GTXCLK	LCD_DE	X2C_RX_DATA7	GPIO45	GPIO45	GPIO45	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[46]	X2C_RX_DATA8	GMAC_PHY_MIITXCLK	LCD_VSYNC	X2C_RX_DATA8	GPIO46	GPIO46	GPIO46	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[47]	X2C_RX_DATA9	GMAC_PHY_TXEN	LCD_HSYNC	X2C_RX_DATA9	GPIO47	GPIO47	GPIO47	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[48]	X2C_RX_DATA10	GMAC_PHY_TXER	LCD_DATA0	X2C_RX_DATA10	GPIO48	GPIO48	GPIO48	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[49]	X2C_RX_DATA11	GMAC_PHY_TXD0	LCD_DATA1	X2C_RX_DATA11	GPIO49	GPIO49	GPIO49	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[50]	X2C_RX_DATA12	GMAC_PHY_TXD1	LCD_DATA2	X2C_RX_DATA12	GPIO50	GPIO50	GPIO50	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[51]	X2C_RX_DATA13	GMAC_PHY_TXD2	LCD_DATA3	X2C_RX_DATA13	GPIO51	GPIO51	GPIO51	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[52]	X2C_RX_DATA14	GMAC_PHY_TXD3	LCD_DATA4	X2C_RX_DATA14	GPIO52	GPIO52	GPIO52	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[53]	X2C_RX_DATA15	GMAC_PHY_TXD4	LCD_DATA5	X2C_RX_DATA15	GPIO53	GPIO53	GPIO53	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[54]	X2C_RX_DATA16	GMAC_PHY_TXD5	LCD_DATA6	X2C_RX_DATA16	GPIO54	GPIO54	GPIO54	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[55]	X2C_RX_DATA17	GMAC_PHY_TXD6	LCD_DATA7	X2C_RX_DATA17	GPIO55	GPIO55	GPIO55	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[56]	X2C_RX_DATA18	GMAC_PHY_TXD7	LCD_DATA8	X2C_RX_DATA18	GPIO56	GPIO56	GPIO56	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[57]	X2C_RX_DATA19	GMAC_PHY_RXCLK	LCD_DATA9	X2C_RX_DATA19	GPIO57	GPIO57	GPIO57	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[58]	X2C_RX_DATA20	GMAC_PHY_RXDV	LCD_DATA10	X2C_RX_DATA20	GPIO58	GPIO58	GPIO58	Disable	Disable	Disable	Disable	Disable

	PAD_FUNC_SHARE[59]	X2C_RX_DATA21	GMAC_PHY_RXER	LCD_DATA11	X2C_RX_DATA21	GPIO59	GPIO59	GPIO59	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[60]	X2C_RX_DATA22	GMAC_PHY_RXD0	LCD_DATA12	X2C_RX_DATA22	GPIO60	GPIO60	GPIO60	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[61]	X2C_RX_DATA23	GMAC_PHY_RXD1	LCD_DATA13	X2C_RX_DATA23	GPIO61	GPIO61	GPIO61	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[62]	X2C_RX_DATA24	GMAC_PHY_RXD2	LCD_DATA14	X2C_RX_DATA24	GPIO62	GPIO62	GPIO62	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[63]	X2C_RX_DATA25	GMAC_PHY_RXD3	LCD_DATA15	X2C_RX_DATA25	GPIO63	GPIO63	GPIO63	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[64]	X2C_RX_DATA26	GMAC_PHY_RXD4	LCD_DATA16	X2C_RX_DATA26	LCD_CLK			Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[65]	X2C_RX_DATA27	GMAC_PHY_RXD5	LCD_DATA17	X2C_RX_DATA27	LCD_DE			Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[66]	X2C_RX_DATA28	GMAC_PHY_RXD6	LCD_DATA18	X2C_RX_DATA28	LCD_VSYNC			Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[67]	X2C_RX_DATA29	GMAC_PHY_RXD7	LCD_DATA19	X2C_RX_DATA29	LCD_HSYNC			Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[68]	X2C_RX_DATA30	GMAC_PHY_CRS	LCD_DATA20	X2C_RX_DATA30	LCD_DATA0			Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[69]	X2C_RX_DATA31	GMAC_PHY_COL	LCD_DATA21	X2C_RX_DATA31	LCD_DATA1			Disable	Disable	Disable	Disable	Disable
LCD	PAD_FUNC_SHARE[70]	LCD_CLK	GMAC_MDC	LCD_DATA22	GPIO0	LCD_DATA2	LCD_CLK	LCD_CLK	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[71]	LCD_DE	GMAC_MDIO	LCD_DATA23	GPIO1	LCD_DATA3	LCD_DE	LCD_DE	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[72]	LCD_VSYNC	X2C_TX_CLK	GPIO0	GPIO2	LCD_DATA4	LCD_VSYNC	LCD_VSYNC	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[73]	LCD_HSYNC	X2C_TX_RST	GPIO1	GPIO3	LCD_DATA5	LCD_HSYNC	LCD_HSYNC	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[74]	LCD_DATA0	X2C_TX_SEND	GPIO2	GPIO4	LCD_DATA6	LCD_DATA0	LCD_DATA0	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[75]	LCD_DATA1	X2C_TX_DATA0	GPIO3	GPIO5	LCD_DATA7	LCD_DATA1	LCD_DATA1	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[76]	LCD_DATA2	X2C_TX_DATA1	GPIO4	GPIO6	LCD_DATA8	LCD_DATA2	LCD_DATA2	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[77]	LCD_DATA3	X2C_TX_DATA2	GPIO5	GPIO7	LCD_DATA9	LCD_DATA3	LCD_DATA3	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[78]	LCD_DATA4	X2C_TX_DATA3	GPIO6	GPIO8	LCD_DATA10	LCD_DATA4	LCD_DATA4	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[79]	LCD_DATA5	X2C_TX_DATA4	GPIO7	GPIO9	LCD_DATA11	LCD_DATA5	LCD_DATA5	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[80]	LCD_DATA6	X2C_TX_DATA5	GPIO8	GPIO10	LCD_DATA12	LCD_DATA6	LCD_DATA6	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[81]	LCD_DATA7	X2C_TX_DATA6	GPIO9	GPIO11	LCD_DATA13	LCD_DATA7	LCD_DATA7	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[82]	LCD_DATA8	X2C_TX_DATA7	GPIO10	GPIO12	LCD_DATA14	LCD_DATA8	LCD_DATA8	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[83]	LCD_DATA9	X2C_TX_DATA8	GPIO11	GPIO13	LCD_DATA15	LCD_DATA9	LCD_DATA9	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[84]	LCD_DATA10	X2C_TX_DATA9	GPIO12	GPIO14	LCD_DATA16	LCD_DATA10	LCD_DATA10	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[85]	LCD_DATA11	X2C_TX_DATA10	GPIO13	GPIO15	LCD_DATA17	LCD_DATA11	LCD_DATA11	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[86]	LCD_DATA12	X2C_TX_DATA11	GPIO14	GPIO16	LCD_DATA18	LCD_DATA12	LCD_DATA12	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[87]	LCD_DATA13	X2C_TX_DATA12	GPIO15	GPIO17	LCD_DATA19	LCD_DATA13	LCD_DATA13	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[88]	LCD_DATA14	X2C_TX_DATA13	GPIO16	GPIO18	LCD_DATA20	LCD_DATA14	LCD_DATA14	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[89]	LCD_DATA15	X2C_TX_DATA14	GPIO17	GPIO19	LCD_DATA21	LCD_DATA15	LCD_DATA15	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[90]	LCD_DATA16	X2C_TX_DATA15	GPIO18	GPIO20	LCD_DATA22	LCD_DATA16	LCD_DATA16	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[91]	LCD_DATA17	X2C_TX_DATA16	GPIO19	GPIO21	LCD_DATA23	LCD_DATA17	LCD_DATA17	Disable	Disable	Disable	Disable	Disable

	PAD_FUNC_SHARE[92]	LCD_DATA18	X2C_TX_DATA17	GPIO20	GPIO22	CM_CLK	LCD_DATA18	LCD_DATA18	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[93]	LCD_DATA19	X2C_TX_DATA18	GPIO21	GPIO23	CM_VSYNC	LCD_DATA19	LCD_DATA19	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[94]	LCD_DATA20	X2C_TX_DATA19	GPIO22	GPIO24	CM_HSYNC	LCD_DATA20	LCD_DATA20	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[95]	LCD_DATA21	X2C_TX_DATA20	GPIO23	GPIO25	CM_DATA0	LCD_DATA21	LCD_DATA21	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[96]	LCD_DATA22	X2C_TX_DATA21	GPIO24	GPIO26	CM_DATA1	LCD_DATA22	LCD_DATA22	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[97]	LCD_DATA23	X2C_TX_DATA22	GPIO25	GPIO27	CM_DATA2	LCD_DATA23	LCD_DATA23	Disable	Disable	Disable	Disable	Disable
CMOS Sensor	PAD_FUNC_SHARE[98]	CM_CLK	X2C_TX_DATA23	GPIO26	GPIO28	CM_DATA3	CM_CLK	CM_CLK	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[99]	CM_VSYNC	X2C_TX_DATA24	GPIO27	GPIO29	CM_DATA4	CM_VSYNC	CM_VSYNC	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[100]	CM_HSYNC	X2C_TX_DATA25	GPIO28	GPIO30	CM_DATA5	CM_HSYNC	CM_HSYNC	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[101]	CM_DATA0	X2C_TX_DATA26	GPIO29	GPIO31	CM_DATA6	CM_DATA0	CM_DATA0	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[102]	CM_DATA1	X2C_TX_DATA27	GPIO30	GPIO32	CM_DATA7	CM_DATA1	CM_DATA1	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[103]	CM_DATA2	X2C_TX_DATA28	GPIO31	GPIO33	CM_DATA8	CM_DATA2	CM_DATA2	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[104]	CM_DATA3	X2C_TX_DATA29	GPIO32	GPIO34	CM_DATA9	CM_DATA3	CM_DATA3	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[105]	CM_DATA4	X2C_TX_DATA30	GPIO33	GPIO35	CM_DATA10	CM_DATA4	CM_DATA4	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[106]	CM_DATA5	X2C_TX_DATA31	GPIO34	GPIO36	CM_DATA11	CM_DATA5	CM_DATA5	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[107]	CM_DATA6	X2C_RX_CLK	GPIO35	GPIO37	CM_DATA12	CM_DATA6	CM_DATA6	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[108]	CM_DATA7	X2C_RX_RST	GPIO36	GPIO38	CM_DATA13	CM_DATA7	CM_DATA7	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[109]	CM_DATA8	X2C_RX_SEND	GPIO37	GPIO39	GMAC_PHY_GTXCLK	CM_DATA8	CM_DATA8	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[110]	CM_DATA9	X2C_RX_DATA0	GPIO38	GPIO40	GMAC_PHY_MIITXCLK	CM_DATA9	CM_DATA9	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[111]	CM_DATA10	X2C_RX_DATA1	GPIO39	GPIO41	GMAC_PHY_TXEN	CM_DATA10	CM_DATA10	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[112]	CM_DATA11	X2C_RX_DATA2	GPIO40	GPIO42	GMAC_PHY_TXER	CM_DATA11	CM_DATA11	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[113]	CM_DATA12	X2C_RX_DATA3	GPIO41	GPIO43	GMAC_PHY_TXD0	CM_DATA12	CM_DATA12	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[114]	CM_DATA13	X2C_RX_DATA4	GPIO42	GPIO44	GMAC_PHY_TXD1	CM_DATA13	CM_DATA13	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[115]	GMAC_PHY_GTXCLK	X2C_RX_DATA5	GPIO43	GPIO45	GMAC_PHY_TXD2	GMAC_PHY_GTXCLK	GMAC_PHY_GTXCLK	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[116]	GMAC_PHY_MIITXCLK	X2C_RX_DATA6	GPIO44	GPIO46	GMAC_PHY_TXD3	GMAC_PHY_MIITXCLK	GMAC_PHY_MIITXCLK	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[117]	GMAC_PHY_TXEN	X2C_RX_DATA7	GPIO45	GPIO47	GMAC_PHY_TXD4	GMAC_PHY_TXEN	GMAC_PHY_TXEN	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[118]	GMAC_PHY_TXER	X2C_RX_DATA8	GPIO46	GPIO48	GMAC_PHY_TXD5	GMAC_PHY_TXER	GMAC_PHY_TXER	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[119]	GMAC_PHY_TXD0	X2C_RX_DATA9	GPIO47	GPIO49	GMAC_PHY_TXD6	GMAC_PHY_TXD0	GMAC_PHY_TXD0	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[120]	GMAC_PHY_TXD1	X2C_RX_DATA10	GPIO48	GPIO50	GMAC_PHY_TXD7	GMAC_PHY_TXD1	GMAC_PHY_TXD1	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[121]	GMAC_PHY_TXD2	X2C_RX_DATA11	GPIO49	GPIO51	GMAC_PHY_RXCLK	GMAC_PHY_TXD2	GMAC_PHY_TXD2	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[122]	GMAC_PHY_TXD3	X2C_RX_DATA12	GPIO50	GPIO52	GMAC_PHY_RXDV	GMAC_PHY_TXD3	GMAC_PHY_TXD3	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[123]	GMAC_PHY_TXD4	X2C_RX_DATA13	GPIO51	GPIO53	GMAC_PHY_RXER	GMAC_PHY_TXD4	GMAC_PHY_TXD4	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[124]	GMAC_PHY_TXD5	X2C_RX_DATA14	GPIO52	GPIO54	GMAC_PHY_RXD0	GMAC_PHY_TXD5	GMAC_PHY_TXD5	Disable	Disable	Disable	Enable	Disable

GMII	PAD_FUNC_SHARE[125]	GMAC_PHY_TXD6	X2C_RX_DATA15	GPIO53	GPIO55	GMAC_PHY_RXD1	GMAC_PHY_TXD6	GMAC_PHY_TXD6	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[126]	GMAC_PHY_TXD7	X2C_RX_DATA16	GPIO54	GPIO56	GMAC_PHY_RXD2	GMAC_PHY_TXD7	GMAC_PHY_TXD7	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[127]	GMAC_PHY_RXCLK	X2C_RX_DATA17	GPIO55	GPIO57	GMAC_PHY_RXD3	GMAC_PHY_RXCLK	GMAC_PHY_RXCLK	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[128]	GMAC_PHY_RXDV	X2C_RX_DATA18	GPIO56	GPIO58	GMAC_PHY_RXD4	GMAC_PHY_RXDV	GMAC_PHY_RXDV	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[129]	GMAC_PHY_RXER	X2C_RX_DATA19	GPIO57	GPIO59	GMAC_PHY_RXD5	GMAC_PHY_RXER	GMAC_PHY_RXER	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[130]	GMAC_PHY_RXD0	X2C_RX_DATA20	GPIO58	GPIO60	GMAC_PHY_RXD6	GMAC_PHY_RXD0	GMAC_PHY_RXD0	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[131]	GMAC_PHY_RXD1	X2C_RX_DATA21	GPIO59	GPIO61	GMAC_PHY_RXD7	GMAC_PHY_RXD1	GMAC_PHY_RXD1	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[132]	GMAC_PHY_RXD2	X2C_RX_DATA22	GPIO60	GPIO62	GMAC_PHY_CRS	GMAC_PHY_RXD2	GMAC_PHY_RXD2	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[133]	GMAC_PHY_RXD3	X2C_RX_DATA23	GPIO61	GPIO63	GMAC_PHY_COL	GMAC_PHY_RXD3	GMAC_PHY_RXD3	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[134]	GMAC_PHY_RXD4	X2C_RX_DATA24	GPIO62	LCD_CLK	GMAC_MDC	GMAC_PHY_RXD4	GMAC_PHY_RXD4	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[135]	GMAC_PHY_RXD5	X2C_RX_DATA25	GPIO63	LCD_DE	GMAC_MDIO	GMAC_PHY_RXD5	GMAC_PHY_RXD5	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[136]	GMAC_PHY_RXD6	X2C_RX_DATA26	X2C_TX_CLK	LCD_VSYNC	X2C_TX_CLK	GMAC_PHY_RXD6	GMAC_PHY_RXD6	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[137]	GMAC_PHY_RXD7	X2C_RX_DATA27	X2C_TX_RST	LCD_HSYNC	X2C_TX_RST	GMAC_PHY_RXD7	GMAC_PHY_RXD7	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[138]	GMAC_PHY_CRS	X2C_RX_DATA28	X2C_TX_SEND	LCD_DATA0	X2C_TX_SEND	GMAC_PHY_CRS	GMAC_PHY_CRS	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[139]	GMAC_PHY_COL	X2C_RX_DATA29	X2C_TX_DATA0	LCD_DATA1	X2C_TX_DATA0	GMAC_PHY_COL	GMAC_PHY_COL	Disable	Disable	Disable	Disable	Disable
	PAD_FUNC_SHARE[140]	GMAC_MDC	X2C_RX_DATA30	X2C_TX_DATA1	LCD_DATA2	X2C_TX_DATA1	GMAC_MDC	GMAC_MDC	Disable	Disable	Disable	Enable	Disable
	PAD_FUNC_SHARE[141]	GMAC_MDIO	X2C_RX_DATA31	X2C_TX_DATA2	LCD_DATA3	X2C_TX_DATA2	GMAC_MDIO	GMAC_MDIO	Disable	Disable	Disable	Enable	Disable
GPIO	PAD_GPIO[0]	U74_JTAG_TDO	GPIO0	X2C_TX_DATA3	LCD_DATA4	X2C_TX_DATA3	PLL_RFSLIP[0]	MIPITX_MPOSV[0]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[1]	U74_JTAG_TCK	GPIO1	X2C_TX_DATA4	LCD_DATA5	X2C_TX_DATA4	PLL_RFSLIP[1]	MIPITX_MPOSV[1]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[2]	U74_JTAG_TDI	GPIO2	X2C_TX_DATA5	LCD_DATA6	X2C_TX_DATA5	PLL_RFSLIP[2]	MIPITX_MPOSV[2]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[3]	U74_JTAG_TMS	GPIO3	X2C_TX_DATA6	LCD_DATA7	X2C_TX_DATA6	PLL_FBSLIP[0]	MIPITX_MPOSV[3]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[4]	U74_JTAG_TRSTN	GPIO4	X2C_TX_DATA7	LCD_DATA8	X2C_TX_DATA7	PLL_FBSLIP[1]	MIPITX_MPOSV[4]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[5]	UART0_RXD	GPIO5	X2C_TX_DATA8	LCD_DATA9	X2C_TX_DATA8	PLL_FBSLIP[2]	MIPITX_MPOSV[5]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[6]	UART0_TXD	GPIO6	X2C_TX_DATA9	LCD_DATA10	X2C_TX_DATA9	PLL0_DIV_OUT	MIPITX_MPOSV[6]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[7]	UART0_CTS	GPIO7	X2C_TX_DATA10	LCD_DATA11	X2C_TX_DATA10	PLL1_DIV_OUT	MIPITX_MPOSV[7]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[8]	UART0_RTS	GPIO8	X2C_TX_DATA11	LCD_DATA12	X2C_TX_DATA11	PLL2_DIV_OUT	MIPITX_MPOSV[8]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[9]	UART0_DCD	GPIO9	X2C_TX_DATA12	LCD_DATA13	X2C_TX_DATA12	DDRPHY_JTAG_TDO[0]	MIPITX_MPOSV[9]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[10]	UART0_RI	GPIO10	X2C_TX_DATA13	LCD_DATA14	X2C_TX_DATA13	DDRPHY_JTAG_TDO[1]	MIPITX_MPOSV[10]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[11]	UART0_DSR	GPIO11	X2C_TX_DATA14	LCD_DATA15	X2C_TX_DATA14	DDRPHY_BIST0_PLL_LOCK[0]	MIPITX_MPOSV[11]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[12]	UART0_DTR	GPIO12	X2C_TX_DATA15	LCD_DATA16	X2C_TX_DATA15	DDRPHY_BIST0_PLL_LOCK[1]	MIPITX_MPOSV[12]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[13]	UART3_RXD	GPIO13	X2C_TX_DATA16	LCD_DATA17	X2C_TX_DATA16	DDRPHY_BIST1_PLL_LOCK[0]	MIPITX_MPOSV[13]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[14]	UART3_TXD	GPIO14	X2C_TX_DATA17	LCD_DATA18	X2C_TX_DATA17	DDRPHY_BIST1_PLL_LOCK[1]	MIPITX_MPOSV[14]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[15]	QSPI_CSN1	GPIO15	X2C_TX_DATA18	LCD_DATA19	X2C_TX_DATA18	DDRPHY_SCAN_EN	MIPITX_MPOSV[15]	Enable	NA	Constant enable	Enable	Constant enable

	PAD_GPIO[16]	QSPI_CSN2	GPIO16	X2C_TX_DATA19	LCD_DATA20	X2C_TX_DATA19	DDRPHY_JTAG_TCK[0]	MIPITX_MPOSV[16]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[17]	QSPI_CSN3	GPIO17	X2C_TX_DATA20	LCD_DATA21	X2C_TX_DATA20	DDRPHY_JTAG_TCK[1]	MIPITX_MPOSV[17]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[18]		GPIO18	X2C_TX_DATA21	LCD_DATA22	X2C_TX_DATA21	DDRPHY_JTAG_TRST[0]	MIPITX_MPOSV[18]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[19]		GPIO19	X2C_TX_DATA22	LCD_DATA23	X2C_TX_DATA22	DDRPHY_JTAG_TRST[1]	MIPITX_MPOSV[19]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[20]		GPIO20	X2C_TX_DATA23	CM_CLK	X2C_TX_DATA23	DDRPHY_JTAG_TMS[0]	MIPITX_MPOSV[20]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[21]		GPIO21	X2C_TX_DATA24	CM_VSYNC	X2C_TX_DATA24	DDRPHY_JTAG_TMS[1]	MIPITX_MPOSV[21]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[22]		GPIO22	X2C_TX_DATA25	CM_HSYNC	X2C_TX_DATA25	DDRPHY_JTAG_TDI[0]	MIPITX_MPOSV[22]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[23]		GPIO23	X2C_TX_DATA26	CM_DATA0	X2C_TX_DATA26	DDRPHY_JTAG_TDI[1]	MIPITX_MPOSV[23]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[24]		GPIO24	X2C_TX_DATA27	CM_DATA1	X2C_TX_DATA27	USBPHY_PIPE_RXIDLE	MIPITX_MPOSV[24]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[25]		GPIO25	X2C_TX_DATA28	CM_DATA2	X2C_TX_DATA28	USBPHY_PIPE_PCLK	MIPITX_MPOSV[25]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[26]		GPIO26	X2C_TX_DATA29	CM_DATA3	X2C_TX_DATA29	USBPHY_LINE_STATE[0]	MIPITX_MPOSV[26]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[27]		GPIO27	X2C_TX_DATA30	CM_DATA4	X2C_TX_DATA30	USBPHY_LINE_STATE[1]	MIPITX_MPOSV[27]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[28]		GPIO28	X2C_TX_DATA31	CM_DATA5	X2C_TX_DATA31	USBPHY_BIST_OK2	MIPITX_MPOSV[28]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[29]	SPI2AHB_CSN	GPIO29	X2C_RX_CLK	CM_DATA6	X2C_RX_CLK	USBPHY_BIST_OK3	MIPITX_MPOSV[29]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[30]	SPI2AHB_SCK	GPIO30	X2C_RX_RST	CM_DATA7	X2C_RX_RST	USBPHY_PWRSTN	MIPITX_MPOSV[30]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[31]	SPI2AHB_D0	GPIO31	X2C_RX_SEND	CM_DATA8	X2C_RX_SEND	USBPHY_TESTMODE	MIPITX_MPOSV[31]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[32]	SPI2AHB_D1	GPIO32	X2C_RX_DATA0	CM_DATA9	X2C_RX_DATA0	USBPHY_PIPE_RSTN	MIPITX_MPOSV[32]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[33]	SPI2AHB_D2	GPIO33	X2C_RX_DATA1	CM_DATA10	X2C_RX_DATA1	USBPHY_HSBIST_MODE	MIPITX_MPOSV[33]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[34]	SPI2AHB_D3	GPIO34	X2C_RX_DATA2	CM_DATA11	X2C_RX_DATA2	USBPHY_CORE_CLKIN	MIPITX_MPOSV[34]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[35]		GPIO35	X2C_RX_DATA3	CM_DATA12	X2C_RX_DATA3	USBPHY_VCONTROL[0]	MIPITX_MPOSV[35]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[36]		GPIO36	X2C_RX_DATA4	CM_DATA13	X2C_RX_DATA4	USBPHY_VCONTROL[1]	MIPITX_MPOSV[36]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[37]		GPIO37	X2C_RX_DATA5	GMAC_PHY_GTXCLK	X2C_RX_DATA5	USBPHY_VCONTROL[2]	MIPITX_MPOSV[37]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[38]		GPIO38	X2C_RX_DATA6	GMAC_PHY_MIITXCLK	X2C_RX_DATA6	USBPHY_VCONTROL[3]	MIPITX_MPOSV[38]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[39]		GPIO39	X2C_RX_DATA7	GMAC_PHY_TXEN	X2C_RX_DATA7	USBPHY_VCONTROL[4]	MIPITX_MPOSV[39]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[40]		GPIO40	X2C_RX_DATA8	GMAC_PHY_TXER	X2C_RX_DATA8	USBPHY_VCONTROL[5]	MIPITX_MPOSV[40]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[41]		GPIO41	X2C_RX_DATA9	GMAC_PHY_TXD0	X2C_RX_DATA9	USBPHY_LSEN	MIPITX_MPOSV[41]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[42]		GPIO42	X2C_RX_DATA10	GMAC_PHY_TXD1	X2C_RX_DATA10	USBPHY_PIPE_TXDEEMPH[0]	MIPITX_MPOSV[42]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[43]		GPIO43	X2C_RX_DATA11	GMAC_PHY_TXD2	X2C_RX_DATA11	USBPHY_PIPE_TXDEEMPH[1]	MIPITX_MPOSV[43]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[44]	VP6_JTAG_TRSTN	GPIO44	X2C_RX_DATA12	GMAC_PHY_TXD3	X2C_RX_DATA12		MIPITX_MPOSV[44]	Enable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[45]	VP6_JTAG_TCK	GPIO45	X2C_RX_DATA13	GMAC_PHY_TXD4	X2C_RX_DATA13		MIPITX_MPOSV[45]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[46]	VP6_JTAG_TMS	GPIO46	X2C_RX_DATA14	GMAC_PHY_TXD5	X2C_RX_DATA14		MIPITX_MPOSV[46]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[47]	VP6_JTAG_TDO	GPIO47	X2C_RX_DATA15	GMAC_PHY_TXD6	X2C_RX_DATA15		MIPITX_DBG_CLK	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[48]	VP6_JTAG_TDI	GPIO48	X2C_RX_DATA16	GMAC_PHY_TXD7	X2C_RX_DATA16		MIPITX_TESTMODE	Disable	NA	Constant enable	Enable	Constant enable

	PAD_GPIO[49]		GPIO49	X2C_RX_DATA17	GMAC_PHY_RXCLK	X2C_RX_DATA17		MIPITX_TEST_RSTN	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[50]		GPIO50	X2C_RX_DATA18	GMAC_PHY_RXDV	X2C_RX_DATA18		MIPITX_RESETB	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[51]		GPIO51	X2C_RX_DATA19	GMAC_PHY_RXER	X2C_RX_DATA19		MIPITX_AON_PWRON_READY_N	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[52]		GPIO52	X2C_RX_DATA20	GMAC_PHY_RXD0	X2C_RX_DATA20		MIPITX_VCONTROL[0]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[53]		GPIO53	X2C_RX_DATA21	GMAC_PHY_RXD1	X2C_RX_DATA21		MIPITX_VCONTROL[1]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[54]		GPIO54	X2C_RX_DATA22	GMAC_PHY_RXD2	X2C_RX_DATA22		MIPITX_VCONTROL[2]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[55]		GPIO55	X2C_RX_DATA23	GMAC_PHY_RXD3	X2C_RX_DATA23		MIPITX_VCONTROL[3]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[56]		GPIO56	X2C_RX_DATA24	GMAC_PHY_RXD4	X2C_RX_DATA24		MIPITX_VCONTROL[4]	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[57]		GPIO57	X2C_RX_DATA25	GMAC_PHY_RXD5	X2C_RX_DATA25		MIPITX_TXCLKESC_ALL	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[58]		GPIO58	X2C_RX_DATA26	GMAC_PHY_RXD6	X2C_RX_DATA26		MIPITX_REFCLK_IN	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[59]		GPIO59	X2C_RX_DATA27	GMAC_PHY_RXD7	X2C_RX_DATA27		MIPITX_PLLSSC_EN	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[60]	BOOT_SEL0(fixed)	GPIO60	X2C_RX_DATA28	GMAC_PHY_CRS	X2C_RX_DATA28		MIPITX_BIST_EN	Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[61]	BOOT_SEL1(fixed)	GPIO61	X2C_RX_DATA29	GMAC_PHY_COL	X2C_RX_DATA29			Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[62]	BOOT_SEL2(fixed)	GPIO62	X2C_RX_DATA30	GMAC_MDC	X2C_RX_DATA30			Disable	NA	Constant enable	Enable	Constant enable
	PAD_GPIO[63]	BOOT_MODE(fixed)	GPIO63	X2C_RX_DATA31	GMAC_MDIO	X2C_RX_DATA31			Disable	NA	Constant enable	Enable	Constant enable

11.1. GPIO FMUX

As an alternate to the pre-defined multiplexed signal groups that can be made available on PAD_FUNC_SHARE and PAD_GPIO signal pads (as listed in Table 11-1 above) a large number of signals can be multiplexed onto the PAD_FUNC_SHARE and PAD_GPIO device pads *when* these pads are configured as GPIOs. So as seen from Table 11-1 when PAD_FUNC_SHARE is configured as Function 4, Function 5 or Function 6 multiplexed signal group then signals GPIO0 - GPIO63 are made available on PAD_FUNC_SHARE[0:63] respectively (these are called *Logical GPIO Pads*.) Similarly when PAD_GPIO is configured as Function 1 multiplexed signal group then signals GPIO0 - GPIO63 are made available on PAD_GPIO[0:63] respectively (these are called *Physical GPIO Pads*.) Note that the GPIO signals appear either on the Physical GPIO pads or the Logical GPIO pads but cannot be configured to appear simultaneously on both of them.

The logical and physical GPIO pads (**from here onwards generically referred to as *GPIO pads or GPIOn pads,* for a specific GPIO pad number *n,* unless explicitly one or the other type is being discussed**) can individually be configured as inputs or outputs through programmable registers. When configured as outputs the corresponding output enables are also configurable through programmable registers. The internal signal sources for the GPIO outputs & enables and the internal signal destinations for the GPIO inputs are listed in the following two tables.

Table 11-2 below lists all the possible internal signal sources for the GPIO pads that can be configured as device outputs and their possible output enables. Note every possible internal signal source which can be configured as a GPIO output doesn't necessarily have a corresponding output enable signal. As such digital 0 and digital 1 is provided which can be selected not just as a possible output data source but more importantly also as an output enable (the output driver enables are active low so selecting a digital 0 will enable the output driver and selecting a digital 1 will disable the output driver.) The output enable signals, if present in the table, can be identified by the trailing *"_OEN"* in the signal name. So for example CPU_JTAG_TDO, at index 3, is an output signal and its corresponding output enable, at index 4, is CPU_JTAG_TDO_*OEN* whereas the signal QSPI_CSN1_OUT at index 47 has no corresponding output enable signal. The index number for an internal signal (data output signal or output enable signal) as listed in this table is used as the value in the appropriate programmable configuration registers (See Section 12.2) to select that specific signal driving out on the GPIO pad.

So by looking at Table 11-1 and Table 11-2 if for example, I2STX_BCLK_OUT is to be made available, on say, PAD_GPIO[10] pad then the following steps are taken:

1. IO_PADSHARE_SEL should be set to 1 to select the Function 1 multiplexed signal group. From Table 10-1 we see that PAD_GPIO[10] for Function 1 is connected to GPIO10.
2. Now looking at Table 11-2 it is seen that the signal I2STX_BCLK_OUT has an index of 21 and I2STX_BCLK_OUT_OEN has an index of 22.

3. Thus the values 21 and 22 are respectively programmed in the two registers associated with GPIO10 pad (see Section 12.2) which makes the signal I2STX_BCLK_OUT available on GPIO10 pad controlled by the output enable signal I2STX_BCLK_OUT_OEN.

Table 11-2 GPIO FMUX Output Data and Output Enable Source Signal List

Index	Signal	Index	Signal	Index	Signal	Index	Signal	Index	Signal	Index	Signal
0	1'b0	23	I2STX_LRCK_OUT	46	PWMDAC_RIGHT_OUT	69	SDIO0_PAD_CDATA_OUT_BIT4	92	SDIO1_PAD_CDATA_OUT_BIT6	115	SPI2AHB_PAD_OE_N_BIT3
1	1'b1	24	I2STX_LRCKOUT_OEN	47	QSPI_CSN1_OUT	70	SDIO0_PAD_CDATA_OUT_BIT5	93	SDIO1_PAD_CDATA_OUT_BIT7	116	SPI2AHB_PAD_TXD_BIT0
2	CLK_GMAC_TOPHYREF	25	I2STX_MCLK_OUT	48	QSPI_CSN2_OUT	71	SDIO0_PAD_CDATA_OUT_BIT6	94	SDIO1_PAD_RST_N	117	SPI2AHB_PAD_TXD_BIT1
3	CPU_JTAG_TDO	26	I2STX_SDOUT0	49	QSPI_CSN3_OUT	72	SDIO0_PAD_CDATA_OUT_BIT7	95	SPDIF_TX_SDOUT	118	SPI2AHB_PAD_TXD_BIT2
4	CPU_JTAG_TDO_OEN	27	I2STX_SDOUT1	50	REGISTER23_SCFG_CMSENSOR_RST0	73	SDIO0_PAD_RST_N	96	SPDIF_TX_SDOUT_OEN	119	SPI2AHB_PAD_TXD_BIT3
5	DMIC_CLK_OUT	28	LCD_PAD_CSM_N	51	REGISTER23_SCFG_CMSENSOR_RST1	74	SDIO1_PAD_CARD_POWER_EN	97	SPI0_PAD_OE_N	120	SPI3_PAD_OE_N
6	DSP_JTDOEN_PAD	29	PWM_PAD_OE_N_BIT0	52	REGISTER32_SCFG_GMAC_PHY_RSTN	75	SDIO1_PAD_CCLK_OUT	98	SPI0_PAD_SCK_OUT	121	SPI3_PAD_SCK_OUT
7	DSP_JTDO_PAD	30	PWM_PAD_OE_N_BIT1	53	SDIO0_PAD_CARD_POWER_EN	76	SDIO1_PAD_CCMD_OE	99	SPI0_PAD_SS_0_N	122	SPI3_PAD_SS_0_N
8	I2C0_PAD_SCK_OE	31	PWM_PAD_OE_N_BIT2	54	SDIO0_PAD_CCLK_OUT	77	SDIO1_PAD_CCMD_OUT	100	SPI0_PAD_SS_1_N	123	SPI3_PAD_SS_1_N
9	I2C0_PAD_SDA_OE	32	PWM_PAD_OE_N_BIT3	55	SDIO0_PAD_CCMD_OE	78	SDIO1_PAD_CDATA_OE_BIT0	101	SPI0_PAD_TXD	124	SPI3_PAD_TXD
10	I2C1_PAD_SCK_OE	33	PWM_PAD_OE_N_BIT4	56	SDIO0_PAD_CCMD_OUT	79	SDIO1_PAD_CDATA_OE_BIT1	102	SPI1_PAD_OE_N	125	UART0_PAD_DTRN
11	I2C1_PAD_SDA_OE	34	PWM_PAD_OE_N_BIT5	57	SDIO0_PAD_CDATA_OE_BIT0	80	SDIO1_PAD_CDATA_OE_BIT2	103	SPI1_PAD_SCK_OUT	126	UART0_PAD_RTSN
12	I2C2_PAD_SCK_OE	35	PWM_PAD_OE_N_BIT6	58	SDIO0_PAD_CDATA_OE_BIT1	81	SDIO1_PAD_CDATA_OE_BIT3	104	SPI1_PAD_SS_0_N	127	UART0_PAD_SOUT
13	I2C2_PAD_SDA_OE	36	PWM_PAD_OE_N_BIT7	59	SDIO0_PAD_CDATA_OE_BIT2	82	SDIO1_PAD_CDATA_OE_BIT4	105	SPI1_PAD_SS_1_N	128	UART1_PAD_SOUT
14	I2C3_PAD_SCK_OE	37	PWM_PAD_OUT_BIT0	60	SDIO0_PAD_CDATA_OE_BIT3	83	SDIO1_PAD_CDATA_OE_BIT5	106	SPI1_PAD_TXD	129	UART2_PAD_DTR_N
15	I2C3_PAD_SDA_OE	38	PWM_PAD_OUT_BIT1	61	SDIO0_PAD_CDATA_OE_BIT4	84	SDIO1_PAD_CDATA_OE_BIT6	107	SPI2_PAD_OE_N	130	UART2_PAD_RTS_N
16	I2SRX_BCLK_OUT	39	PWM_PAD_OUT_BIT2	62	SDIO0_PAD_CDATA_OE_BIT5	85	SDIO1_PAD_CDATA_OE_BIT7	108	SPI2_PAD_SCK_OUT	131	UART2_PAD_SOUT
17	I2SRX_BCLK_OUT_OEN	40	PWM_PAD_OUT_BIT3	63	SDIO0_PAD_CDATA_OE_BIT6	86	SDIO1_PAD_CDATA_OUT_BIT0	109	SPI2_PAD_SS_0_N	132	UART3_PAD_SOUT
18	I2SRX_LRCK_OUT	41	PWM_PAD_OUT_BIT4	64	SDIO0_PAD_CDATA_OE_BIT7	87	SDIO1_PAD_CDATA_OUT_BIT1	110	SPI2_PAD_SS_1_N	133	USB_DRV_BUS
19	I2SRX_LRCK_OUT_OEN	42	PWM_PAD_OUT_BIT5	65	SDIO0_PAD_CDATA_OUT_BIT0	88	SDIO1_PAD_CDATA_OUT_BIT2	111	SPI2_PAD_TXD		
20	I2SRX_MCLK_OUT	43	PWM_PAD_OUT_BIT6	66	SDIO0_PAD_CDATA_OUT_BIT1	89	SDIO1_PAD_CDATA_OUT_BIT3	112	SPI2AHB_PAD_OE_N_BIT0		
21	I2STX_BCLK_OUT	44	PWM_PAD_OUT_BIT7	67	SDIO0_PAD_CDATA_OUT_BIT2	90	SDIO1_PAD_CDATA_OUT_BIT4	113	SPI2AHB_PAD_OE_N_BIT1		
22	I2STX_BCLK_OUT_OEN	45	PWMDAC_LEFT_OUT	68	SDIO0_PAD_CDATA_OUT_BIT3	91	SDIO1_PAD_CDATA_OUT_BIT5	114	SPI2AHB_PAD_OE_N_BIT2		

The following table lists all the possible internal signal destinations for the GPIO inputs. If the signal is present in this table (the index number is not relevant) then it means there is an appropriate programmable configuration registers (see Section 12.3) to select that specific signal as the destination for a specific GPIO input. Table 11-2 still provides the signals for controlling the output enables. If the output enable signal doesn't exist then the pad is purely an input and the corresponding output enable configuration register is set to 0x1 thus disabling the output driver (output driver enable is active low.)

If for example, CPU_JTAG_TCK (an input to the device) is to be made available, on say GPIO10 device pad then by looking at Table 11-1, Table 11-2 and Table 11-3 the following steps are taken:

1. IO_PADSHARE_SEL should be set to 1 to select the Function 1 multiplexed signal group. Table 10-1 shows that PAD_GPIO[10] for Function 1 is connected to GPIO10.
2. Table 11-3 indicates (at index 1) that CPU_JTAG_TCK is a valid signal to receive an input from a GPIO pad. As such the configuration register associated with this signal (see Section 12.3) is programmed with the index of the GPIO10 (0xC - 2 + 10 = 12.)
3. Furthermore Table 11-2 indicates that there is no output enable signal associated with this signal (no signal by the name CPU_JTAG_TCK_OEN). As such the output enable configuration register for GPIO10 is set to 0x1 (Output is disabled.)

Table 11-3 GPIO FMUX Input Data Destination Signal List

Index	Signal	Index	Signal	Index	Signal	Index	Signal	Index	Signal
1	CPU_JTAG_TCK	16	I2C2_PAD_SDA_IN	31	SDIO0_PAD_CDATA_IN_BIT2	46	SDIO1_PAD_CDATA_IN_BIT6	61	SPI3_PAD_RXD
2	CPU_JTAG_TDI	17	I2C3_PAD_SCK_IN	32	SDIO0_PAD_CDATA_IN_BIT3	47	SDIO1_PAD_CDATA_IN_BIT7	62	SPI3_PAD_SS_IN_N
3	CPU_JTAG_TMS	18	I2C3_PAD_SDA_IN	33	SDIO0_PAD_CDATA_IN_BIT4	48	SPDIF_RX_SDIN	63	UART0_PAD_CTSN
4	CPU_JTAG_TRST	19	I2SRX_BCLK_IN	34	SDIO0_PAD_CDATA_IN_BIT5	49	SPI0_PAD_RXD	64	UART0_PAD_DCDN
5	DMIC_SDIN_BIT0	20	I2SRX_LRCK_IN	35	SDIO0_PAD_CDATA_IN_BIT6	50	SPI0_PAD_SS_IN_N	65	UART0_PAD_DSRN
6	DMIC_SDIN_BIT1	21	I2SRX_SDIN_BIT0	36	SDIO0_PAD_CDATA_IN_BIT7	51	SPI1_PAD_RXD	66	UART0_PAD_RIN
7	DSP_JTCK_PAD	22	I2SRX_SDIN_BIT1	37	SDIO1_PAD_CARD_DETECT_N	52	SPI1_PAD_SS_IN_N	67	UART0_PAD_SIN
8	DSP_JTDI_PAD	23	I2SRX_SDIN_BIT2	38	SDIO1_PAD_CARD_WRITE_PRT	53	SPI2_PAD_RXD	68	UART1_PAD_SIN
9	DSP_JTMS_PAD	24	I2STX_BCLK_IN	39	SDIO1_PAD_CCMD_IN	54	SPI2_PAD_SS_IN_N	69	UART2_PAD_CTS_N
10	DSP_TRST_PAD	25	I2STX_LRCK_IN	40	SDIO1_PAD_CDATA_IN_BIT0	55	SPI2AHB_PAD_RXD_BIT0	70	UART2_PAD_DCD_N
11	I2C0_PAD_SCK_IN	26	SDIO0_PAD_CARD_DETECT_N	41	SDIO1_PAD_CDATA_IN_BIT1	56	SPI2AHB_PAD_RXD_BIT1	71	UART2_PAD_DSR_N
12	I2C0_PAD_SDA_IN	27	SDIO0_PAD_CARD_WRITE_PRT	42	SDIO1_PAD_CDATA_IN_BIT2	57	SPI2AHB_PAD_RXD_BIT2	72	UART2_PAD_RI_N
13	I2C1_PAD_SCK_IN	28	SDIO0_PAD_CCMD_IN	43	SDIO1_PAD_CDATA_IN_BIT3	58	SPI2AHB_PAD_RXD_BIT3	73	UART2_PAD_SIN
14	I2C1_PAD_SDA_IN	29	SDIO0_PAD_CDATA_IN_BIT0	44	SDIO1_PAD_CDATA_IN_BIT4	59	SPI2AHB_PAD_SS_N	74	UART3_PAD_SIN
15	I2C2_PAD_SCK_IN	30	SDIO0_PAD_CDATA_IN_BIT1	45	SDIO1_PAD_CDATA_IN_BIT5	60	SPI2AHB_SLV_SCLKIN	75	USB_OVER_CURRENT

Explanation for the next table is TBD

Table 11-4 Signal Full MUX with GPIO Description

Interface	Signal Name	Function Description	Direction	Width	GPIO Reuse default Function	
					PU Configure	Default GPIO Pad
U74 JTAG	CPU_JTAG_TRSTN	JTAG reset, low active	I	1		GPIO4
	CPU_JTAG_TCK	JTAG clock	I	1	PU	GPIO1
	CPU_JTAG_TMS	JTAG mode select	I	1		GPIO3
	CPU_JTAG_TDO	JTAG data output	O	1		GPIO0
	CPU_JTAG_TDI	JTAG data input	I	1		GPIO2
VP6 JTAG	VP6_JTAG_TRSTN	JTAG reset, low active	I	1	PU	GPIO44
	VP6_JTAG_TCK	JTAG clock	I	1		GPIO45
	VP6_JTAG_TMS	JTAG mode select	I	1		GPIO46
	VP6_JTAG_TDO	JTAG data output	O	1		GPIO47
	VP6_JTAG_TDI	JTAG data input	I	1		GPIO48
ADSP JTAG	ADSP_JTAG_TRSTN	JTAG reset, low active	I	1		
	ADSP_JTAG_TCK	JTAG clock	I	1		
	ADSP_JTAG_TMS	JTAG mode select	I	1		
	ADSP_JTAG_TDO	JTAG data output	O	1		
	ADSP_JTAG_TDI	JTAG data input	I	1		
E24 JTAG	E24_JTAG_TRSTN	JTAG reset, low active	I	1		
	E24_JTAG_TCK	JTAG clock	I	1		
	E24_JTAG_TMS	JTAG mode select	I	1		
	E24_JTAG_TDO	JTAG data output	O	1		
	E24_JTAG_TDI	JTAG data input	I	1		
Audio	SPDIF_DATA	SPDIF in/out data	B	1		
	PWMDAC_LEFT	PWM DAC left channel wave	O	1		
	PWMDAC_RIGHT	PWM DAC right channel wave	O	1		
	I2S_TX_MCLK	I2S audio codec main clock	O	1		
	I2S_TX_BCLK	I2S transmitter bit clock for audio DAC	B	1		
	I2S_TX_LRCK	I2S transmitter L/R flag for audio DAC	B	1		
	I2S_TX_SDOUT0	I2S transmitter serial data output to audio DAC	O	1		
	I2S_TX_SDOUT1	I2S transmitter serial data output to audio DAC	O	1		
	I2S_RX_MCLK	I2S audio codec main clock	O	1		
	I2S_RX_BCLK	I2S RX bit clock to audio ADC	B	1		
	I2S_RX_LRCK	I2S RX L/R flag to audio ADC	B	1		
	I2S_RX_SDIN0	I2S RX serial data input from audio ADC	I	1		
	I2S_RX_SDIN1	I2S RX serial data input from audio ADC	I	1		
	I2S_RX_SDIN2	I2S RX serial data input from audio ADC	I	1		
	DMIC_CLK	PDM clock output to DMIC	O	1		
	DMIC_DIN0	PDM serial data input from DMIC	I	1		
	DMIC_DIN1	PDM serial data input from DMIC	I	1		
SDIO 0	SDIO0_CCLK	card clock output	O	1		
	SDIO0_RSTN	reset for external eMMC	O	1		
	SDIO0_CCMD	card command	B	1		
	SDIO0_CDATA[7:0]	card data	B	8		
	SDIO0_C_DETECTED	card detected	I	1		
	SDIO0_C_WRITE_PRT	card write protected status	I	1		
	SDIO0_PWR_EN	card power enable	O	1		

Interface	Signal Name	Function Description	Direction	Width	GPIO Reuse default Function	
					PU Configure	Default GPIO Pad
SDIO 1	SDIO1_CCLK	card clock output	O	1		
	SDIO1_RSTN	reset for external eMMC	O	1		
	SDIO1_CCMD	card command	B	1		
	SDIO1_CDATA[7:0]	card data	B	8		
	SDIO1_C_DETECTED	card detected	I	1		
	SDIO1_C_WRITE_PRT	card write protected status	I	1		
	SDIO1_PWR_EN	card power enable	O	1		
SPI0	SPI0_SCLK	SPI0 clock	O	1		
	SPI0_TXD	SPI0 data output	O	1		
	SPI0_RXD	SPI0 data input	I	1		
	SPI0_CSN0	SPI0 chip select 0, low active	O	1		
	SPI0_CSN1	SPI0 chip select 1,low active	O	1		
SPI1	SPI1_SCLK	SPI1 clock	O	1		
	SPI1_TXD	SPI1 data output	O	1		
	SPI1_RXD	SPI1 data input	I	1		
	SPI1_CSN0	SPI1 chip select 0, low active	O	1		
	SPI1_CSN1	SPI1 chip select 1,low active	O	1		
SPI2	SPI2_SCLK	SPI2 clock	O	1		
	SPI2_TXD	SPI2 data output	O	1		
	SPI2_RXD	SPI2 data input	I	1		
	SPI2_CSN0	SPI2 chip select 1, low active	O	1		
	SPI2_CSN1	SPI2 chip select 2,low active	O	1		
SPI3	SPI3_SCLK	SPI3 clock	O	1		
	SPI2_TXD	SPI3 data output	O	1		
	SPI3_RXD	SPI3 data input	I	1		
	SPI3_CSN0	SPI3 chip select 1, low active	O	1		
	SPI3_CSN1	SPI3 chip select 2,low active	O	1		
SPI2AHB	SPI2AHB_CSN	SPI chip select , low active	I	1		GPIO29
	SPI2AHB_SCK	SPI clock	I	1		GPIO30
	SPI2AHB_D0	SPI data 0	B	1		GPIO31
	SPI2AHB_D1	SPI data 1	B	1		GPIO32
	SPI2AHB_D2	SPI data 2	B	1		GPIO33
	SPI2AHB_D3	SPI data 3	B	1		GPIO34
I2C0	I2C0_SDA	I2C0 serial data	B	1		
	I2C0_SCL	I2C0 serial clock	B	1		
I2C1	I2C1_SDA	I2C1 serial data	B	1		
	I2C1_SCL	I2C1 serial clock	B	1		
I2C2	I2C2_SDA	I2C2 serial data	B	1		
	I2C2_SCL	I2C2 serial clock	B	1		
I2C3	I2C3_SDA	I2C3 serial data	B	1		
	I2C3_SCL	I2C3 serial clock	B	1		
UART0	UART0_RXD	UART0 receive data	I	1	PU	GPIO5
	UART0_TXD	UART0 transmit data	O	1	PU	GPIO6
	UART0_CTS	UART0 Clear To Send modem status	I	1		GPIO7
	UART0_RTS	UART0 modem Control Request To Send output	O	1		GPIO8
	UART0_DCD	UART0 data carrier detect modem status input	I	1		GPIO9

Interface	Signal Name	Function Description	Direction	Width	GPIO Reuse default Function	
					PU Configure	Default GPIO Pad
	UART0_RI	UART0 ring indicator status input	I	1		GPIO10
	UART0_DSR	UART0 data set ready modem status input	I	1		GPIO11
	UART0_DTR	UART0 modem control data terminal ready output	O	1		GPIO12
UART1	UART1_RXD	UART1 receive data	I	1		
	UART1_TXD	UART1 transmit data	O	1		
UART2	UART2_RXD	UART2 receive data	I	1		
	UART2_TXD	UART2 transmit data	O	1		
	UART2_CTS	UART2 Clear To Send modem status	I	1		
	UART2_RTS	UART2 modem Control Request To Send output	O	1		
	UART2_DCD	UART2 data carrier detect modem status input	I	1		
	UART2_RI	UART2 ring indicator status input	I	1		
	UART2_DSR	UART2 data set ready modem status input	I	1		
	UART2_DTR	UART2 modem control data terminal ready output	O	1		
UART3	UART3_RXD	UART3 receive data	I	1	PU	GPIO13
	UART3_TXD	UART3 transmit data	O	1	PU	GPIO14
PWM	PWM_OUT0	PWM channel0 output	O	1		
	PWM_OUT1	PWM channel1 output	O	1		
	PWM_OUT2	PWM channel2 output	O	1		
	PWM_OUT3	PWM channel3 output	O	1		
	PWM_OUT4	PWM channel4 output	O	1		
	PWM_OUT5	PWM channel5 output	O	1		
	PWM_OUT6	PWM channel6 output	O	1		
	PWM_OUT7	PWM channel7 output	O	1		
CMOS Sensor (BT656, BT1120, DVP)	CM_RST0	sensor reset	O	1		
	CM_RST1	sensor reset	O	1		
GMII	GMAC_PHY_CLK	GMAC PHY clock	O	1		
	GMAC_PHY_RSTN	GMAC PHY reset	O	1		
QSPI	QSPI_CSN1	Flash chip select 1, low active	O	1	PU	GPIO15
	QSPI_CSN2	Flash chip select 1, low active	O	1	PU	GPIO16
	QSPI_CSN3	Flash chip select 1, low active	O	1	PU	GPIO17
LCD	LCD_CSM_N	LCD 80 interface CS_N	O	1		
USB	USB_DRV_BUS	Drive vbus	O	1		
	USB_OVER_CURRENT	Overcurrent detected	I	1		
BOOT SEL	BOOT_SEL0	boot select 0	I	1		GPIO60
	BOOT_SEL1	boot select 1	I	1		GPIO61
	BOOT_SEL2	boot select 2	I	1		GPIO62
	BOOT_MODE	boot mode	I	1		GPIO63

12. GPIO Configuration Registers

In this chapter the configuration registers associated with GPIO pads are defined. The registers are described in the following three sections:

1. Configuration registers for GPIO interrupts (Section 12.1).
2. Registers for configuring GPIOs as outputs for IP blocks (Section 12.2).
3. Registers for configuring GPIOs as inputs for IP blocks (Section 12.3).

As described in Chapter 11 GPIO pads, based on device configuration, are available on either the PAD_GPIO or the PAD_FUNC_SHARE device pads (shown in Table 11-1). All the *GPIO Configuration Registers*, defined in this chapter, are applicable to GPIO pads independent of whether they are PAD_GPIO or PAD_FUNC_SHARE device pads.

12.1. Configuration Registers for GPIO Interrupts

This section defines all the configuration registers related to GPIO interrupts. An interrupt is associated with each GPIO pad. Each interrupt can individually be configured as follows:

1. It can be enabled or disabled.
2. It can be edge-triggered or level-triggered
3. Edge-triggered interrupts can be configured to trigger on a positive edge or negative edge or both edges.
4. Level-triggered interrupts can be configured to trigger on a high-level signal or a low-level signal
5. It can be masked.
6. Both raw interrupts and masked interrupts are available.
7. It can be cleared.

Globally all interrupts can be enabled or disabled through a single configuration register.

Table 12-1 Global Enable for GPIO Interrupts

GPIOEN: Global Enable for GPIO Interrupts				
Offset Address		**0x0**		
Bit	**Field**	**Type**	**Reset**	**Description**
[0]	GPIOEN	R/W	0x0	Globally enables all the GPIO interrupts. If set to 1 the GPIO interrupts are enabled. If set to 0 the GPIO interrupts are disabled.
[31:1]	Reserved	R/W	0x0	Writes are ignored and reads return a 0.

Table 12-2 Interrupt Type for GPIO[31:0]

GPIOIS_0: Interrupt Type for GPIO[31:0]				
Offset Address		**0x10**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOS_0	R/W	0x0	Selects if individual GPIO interrupts are edge-triggered or level-triggered. If set to 1 the interrupt is edge-triggered. If set to 0 the interrupt is level-triggered. GPIOS_0[0] is for GPIO[0], GPIOS_0[1] is for GPIO[1], … and GPIOS_1[31] is for GPIO[31].

Table 12-3 Interrupt Type for GPIO[63:32]

GPIOIS_1: Interrupt Type for GPIO[63:32]				
Offset Address		**0x14**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOS_1	R/W	0x0	Selects if individual GPIO interrupts are edge-triggered or level-triggered. If set to 1 the interrupt is edge-triggered. If set to 0 the interrupt is level-triggered. GPIOS_1[0] is for GPIO[32], GPIOS_1[1] is for GPIO[33], … and GPIOS_1[31] is for GPIO[63].

Table 12-4 Edge-Trigger Interrupt Type for GPIO[31:0]

GPIOIBE_0: Edge-Trigger Interrupt Type for GPIO[31:0]				
Offset Address		**0x18**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIBE_0	R/W	0x0	Effective when the corresponding GPIOS_1 is set to a 1 i.e., the interrupt is edge-triggered. If set to 1 the interrupt gets triggered on both positive & negative edges. If set to 0 the interrupt is triggered by a single edge (polarity of single edge determined by GPIOIEV_0 [31:0] shown below.) GPIOBE_0[0] is for GPIO[0], GPIOBE_0[1] is for GPIO[1], … and GPIOBE_1[31] is for GPIO[31].

Table 12-5 Edge-Trigger Interrupt Type for GPIO[63:32]

GPIOIBE_1: GPIO Edge-Trigger Interrupt Type for GPIO[63:32]				
Offset Address		**0x1C**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIBE_1	R/W	0x0	Effective when the corresponding GPIOS_1 is set to a 1 i.e., the interrupt is edge-triggered. If set to 1 the interrupt gets triggered on both positive & negative edges. If set to 0 the interrupt is triggered by a single edge (polarity of single edge determined by GPIOIEV_1 [31:0] shown below.) GPIOBE_1[0] is for GPIO[32], GPIOBE_1[1] if for GPIO[32], … and GPIOBE_1[31] is for GPIO[63].

Table 12-6 Interrupt Trigger Polarity for GPIO[31:0]

GPIOIEV_0: Interrupt Trigger Polarity for GPIO[31:0]				
Offset Address		**0x20**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIEV_0	R/W	0x0	Determines the polarity of the signal on which the interrupt is triggered. If it is set to 1 then the interrupt is triggered either on a rising edge (edge-triggered) or high-level (level-triggered). If it is set to 0 then the interrupt is triggered either on a falling edge (edge-triggered) or low-level (level-triggered). If the interrupt is edge-triggered and the corresponding GPIOBE_0 bit is set to 1 (triggered by both rising & falling edges) then this bit is ignored. GPIOEV_0[0] is for GPIO[0], GPIOEV_0[1] is for GPIO[1], … and GPIOEV_0[31] is for GPIO[31].

Table 12-7 Interrupt Trigger Polarity for GPIO[63:32]

GPIOIEV_1: Interrupt Trigger Polarity for GPIO[63:32]				
Offset Address		**0x24**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIEV_0	R/W	0x0	Determines the polarity of the signal on which the interrupt is triggered. If it is set to 1 then the interrupt is triggered either on a rising edge (edge-triggered) or high-level (level-triggered). If it is set to 0 then the interrupt is triggered either on a falling edge (edge-triggered) or low-level (level-triggered). If the interrupt is edge-triggered and the corresponding GPIOBE_1 bit is set to 1 (triggered by both rising & falling edges) then this bit is ignored. GPIOEV_1[0] is for GPIO[32], GPIOEV_1[1] is for GPIO[33], … and GPIOEV_1[31] is for GPIO[63].

Table 12-8 Interrupt Mask for GPIO[31:0]

GPIOIE_0: Interrupt Mask for GPIO[31:0]				
Offset Address		**0x28**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIE_0	R/W	0x0	If set to 1 the corresponding interrupt is disabled (masked). If set to 0 the corresponding interrupt is enabled (unmasked). GPIOIE_0[0] is for GPIO[0], GPIOIE_0[1] is for GPIO[1], … and GPIOIE_0[31] is for GPIO[31].

Table 12-9 Interrupt Mask for GPIO [61:32]

GPIOIE_1: Interrupt Mask for GPIO[63:32]				
Offset Address		**0x2C**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIE_1	R/W	0x0	If set to 1 the corresponding interrupt is disabled (masked). If set to 0 the corresponding interrupt is enabled (unmasked). GPIOIE_1[0] is for GPIO[32], GPIOIE_1[1] is for GPIO[33], … and GPIOIE_1[31] is for GPIO[63].

Table 12-10 Clear Edge-Triggered Interrupts for GPIO [31:0]

GPIOIC_0: Clear Edge-Triggered Interrupts for GPIO[31:0]				
Offset Address		**0x30**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIC_0	R/W	0x0	Write a 1 to clear the edge-triggered interrupt. GPIOIC_0[0] is for GPIO[0], GPIOIC_0[1] is for GPIO[1], … and GPIOIC_0[31] is for GPIO[31].

Table 12-11 Clear Edge-Triggered Interrupts for GPIO [63:32]

GPIOIC_1: Clear Edge-Triggered Interrupts for GPIO[63:32]				
Offset Address		**0x34**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOIC_1	R/W	0x0	Write a 1 to clear the edge-triggered interrupt. GPIOIC_1[0] is for GPIO[32], GPIOIC_1[1] is for GPIO[33], … and GPIOIC_1[31] is for GPIO[63]

Table 12-12 Edge-Triggered Interrupt Status for GPIO [31:0]

GPIORIS_0: Edge-Triggered Interrupt Status for GPIO[31:0]				
Offset Address		**0x38**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIORIS_0	R	0x0	Provides the status of an edge-triggered interrupt. If 1 then it means that the edge, as configured, was detected. If 0 then it means that the edge, as configured, was not detected. GPIOIRIS_0[0] is for GPIO[0], GPIOIRIS_0[1] is for GPIO[1], … and GPIOIRIS_0[31] is for GPIO[31].

Table 12-13 Edge-Triggered Interrupt Status for GPIO [61:32]

GPIORIS_1: Edge-Triggered Interrupt Status for GPIO[61:32]				
Offset Address		**0x3C**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIORIS_1	R	0x0	Provides the status of an edge-triggered interrupt. If 1 then it means that the edge, as configured, was detected. If 0 then it means that the edge, as configured, was not detected. GPIOIRIS_1[0] is for GPIO[32], GPIOIRIS_1[1] is for GPIO[33], … and GPIOIRIS_1[31] is for GPIO[63].

Table 12-14 Interrupt Status after Masking for GPIO[31:0]

GPIOMIS_0: Interrupt Status after Masking for GPIO[31:0]				
Offset Address		**0x40**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOMIS_0	R	0x0	Provides the status of an edge-triggered or a level-triggered interrupt after masking. If 1 then it means that the edge or level, as configured, was detected. If 0 then it means that the edge or level, as configured, was not detected. GPIOIMIS_0[0] is for GPIO[0], GPIOIMIS_0[1] is for GPIO[1], … and GPIOIMIS_0[31] is for GPIO[31].

Table 12-15 Interrupt Status after Masking for GPIO [61:32]

GPIOMIS_1: Interrupt Status after Masking for GPIO[61:32]				
Offset Address		**0x44**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIOMIS_1	R	0x0	Provides the status of an edge-triggered or a level-triggered interrupt after masking. If 1 then it means that the edge or level, as configured, was detected. If 0 then it means that the edge or level, as configured, was not detected. GPIOIMIS_1[0] is for GPIO[32], GPIOIMIS_1[1] is for GPIO[33], … and GPIOIMIS_1[31] is for GPIO[63].

Table 12-16 Data Value of GPIO [31:0]

GPIODIN_0: Data Value of GPIO[31:0]				
Offset Address		**0x48**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIODIN_0	R	0x0	Dynamically reflects the value on the GPIO pin. If 1 the pin is a digital 1 and if 0 the pin is a digital 0. GPIODIN_0[0] is for GPIO[0], GPIODIN_0[1] is for GPIO[1], … and GPIODIN_0[31] is for GPIO[31].

Table 12-17 Data Value of GPIO [61:32]

GPIODIN_1: Data Value of GPIO[63:32]				
Offset Address		**0x4C**		
Bit	**Field**	**Type**	**Reset**	**Description**
[31:0]	GPIODIN_1	R	0x0	Dynamically reflects the value on the GPIO pin. If 1 the pin is a digital 1 and if 0 the pin is a digital 0. GPIODIN_1[0] is for GPIO[32], GPIODIN_1[1] is for GPIO[33], … and GPIODIN_1[31] is for GPIO[63].

12.2. Registers for Configuring GPIOs as Outputs for IP Block Signals

Since there are 64 GPIO pads, each of which can be configured as an output, there are 64 *Output Data* configuration registers, one for each GPIO pad. Programming these registers determines which of the internal signal will get connected to a particular GPIO output driver.

Similarly there are 64 *Output Enable* configuration registers, one for each GPIO pad. Programming these registers controls the output enable of these output drivers. Individual output enable control is provided so that an output enable can be disabled (statically) if the GPIO is configured as an input or get dynamically changed as need be by connecting to some internal signal.

These 128 registers are concisely defined in this section in a single table. There are a pair of entries for the output data and the output enable signals for each GPIO pad. As such the first entry in the table is for register GPO**0**_DOUT_CFG which is the output data configuration register for GPIO**0**, the third entry GPO**1**_DOUT_CFG is the output data configuration register for GPIO**1** and so on with every alternate entry being the output data configuration register for subsequent GPIO pads all the way down to the 127th entry which is GPO**63**_DOUT_CFG for GPIO**63**. Similarly the second entry in the table is for register GPO**0**_DOEN_CFG which is the output enable configuration register for GPIO**0**, the fourth entry GPO**1**_DOEN_CFG is the output enable configuration register for GPIO**1** and so on with every alternate entry being the output enable configuration register for subsequent GPIO pads all the way down to the 128th entry which is GPO**63**_DOEN_CFG for GPIO**63**.

As described in Table 11-2 there are a total of 133 internal signals (including a digital 0 and a digital 1) which can be used for providing either the actual data which is driven out or provide an output enable for the output driver. Note every output signal in the table does not have a corresponding output enable signal.

Each configuration register has two fields:

1. The first field, which is a single bit (bit 31), is a *Bit Reverse* field. If the bit is 1 then the signal selected by the second field is inverted before it is used either as the output data or as the enable signal. If it is 0 no inversion takes place.
2. The value loaded in the second field (bits 30:0) is the index value of the signal from Table 11-2. The index value loaded in the Output Data register's field makes the corresponding signal appear on the output of the GPIO pad. The index value loaded in the Output Enable register's field makes the corresponding signal control the output enable of the GPIO pad.

As an example let's look at the case of driving SDIO0_PAD_CCMD_OUT on GPIO0 pad. The index for this signal in Table 11-2 is 56 (0x38). There is a corresponding output enable signal SDIO0_PAD_CCMD_OE at index 55 (0x37) which is an active high signal. Signal inversion is required for the output enable signal to make it an active low signal. So the values loaded in the configuration registers for GPIO0 are as follows:

```
GPO0_DOUT_CFG[GPO0_DOUT_BIT_REVERSE] = 0x0;          //No bit reversal
GPO0_DOUT_CFG[GPO0_DOUT_CFG]  = 0x38;                //The index number for the signal from the table
GPO0_DOEN_CFG[GPO0_DOEN_BIT_REVERSE] = 0x1;          //Bit reversal active to make the signal active low
GPO0_DOEN_CFG[GPO0_DOEN_CFG]  = 0x37;                //Output enabled by default since no enable signal
```

If there was no corresponding output enable signal in the table then the value loaded in the output enable configurations registers would be as follows:

```
GPO0_DOEN_CFG[GPO0_DOEN_BIT_REVERSE] = 0x0;          //No bit reversal
GPO0_DOEN_CFG[GPO0_DOEN_CFG]  = 0x0;                 //Active Low output enable
```

Table 12-18 Registers for Configuring GPIOs as Outputs

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
GPO0_DOUT_CFG	0x50	[31]	GPO0_DOUT_BIT_REVERSE	R/W	0x0	GPIO0
		[30:0]	GPO0_DOUT_CFG		0x3	
GPO0_DOEN_CFG	0x54	[31]	GPO0_DOEN_BIT_REVERSE	R/W	0x0	GPIO0
		[30:0]	GPO0_DOEN_CFG		0x4	
GPO1_DOUT_CFG	0x58	[31]	GPO1_DOUT_BIT_REVERSE	R/W	0x0	GPIO1
		[30:0]	GPO1_DOUT_CFG		0x0	
GPO1_DOEN_CFG	0x5C	[31]	GPO1_DOEN_BIT_REVERSE	R/W	0x0	GPIO1
		[30:0]	GPO1_DOEN_CFG		0x1	
GPO2_DOUT_CFG	0x60	[31]	GPO2_DOUT_BIT_REVERSE	R/W	0x0	GPIO2
		[30:0]	GPO2_DOUT_CFG		0x0	
GPO2_DOEN_CFG	0x64	[31]	GPO2_DOEN_BIT_REVERSE	R/W	0x0	GPIO2
		[30:0]	GPO2_DOEN_CFG		0x1	
GPO3_DOUT_CFG	0x68	[31]	GPO3_DOUT_BIT_REVERSE	R/W	0x0	GPIO3
		[30:0]	GPO3_DOUT_CFG		0x0	
GPO3_DOEN_CFG	0x6C	[31]	GPO3_DOEN_BIT_REVERSE	R/W	0x0	GPIO3
		[30:0]	GPO3_DOEN_CFG		0x1	
GPO4_DOUT_CFG	0x70	[31]	GPO4_DOUT_BIT_REVERSE	R/W	0x0	GPIO4
		[30:0]	GPO4_DOUT_CFG		0x0	
GPO4_DOEN_CFG	0x74	[31]	GPO4_DOEN_BIT_REVERSE	R/W	0x0	GPIO4
		[30:0]	GPO4_DOEN_CFG		0x1	
GPO5_DOUT_CFG	0x78	[31]	GPO5_DOUT_BIT_REVERSE	R/W	0x0	GPIO5

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO5_DOUT_CFG		0x0	
GPO5_DOEN_CFG	0x7C	[31]	GPO5_DOEN_BIT_REVERSE	R/W	0x0	GPIO5
		[30:0]	GPO5_DOEN_CFG		0x1	
GPO6_DOUT_CFG	0x80	[31]	GPO6_DOUT_BIT_REVERSE	R/W	0x0	GPIO6
		[30:0]	GPO6_DOUT_CFG		0x7F	
GPO6_DOEN_CFG	0x84	[31]	GPO6_DOEN_BIT_REVERSE	R/W	0x0	GPIO6
		[30:0]	GPO6_DOEN_CFG		0x0	
GPO7_DOUT_CFG	0x88	[31]	GPO7_DOUT_BIT_REVERSE	R/W	0x0	GPIO7
		[30:0]	GPO7_DOUT_CFG		0x0	
GPO7_DOEN_CFG	0x8C	[31]	GPO7_DOEN_BIT_REVERSE	R/W	0x0	GPIO7
		[30:0]	GPO7_DOEN_CFG		0x1	
GPO8_DOUT_CFG	0x90	[31]	GPO8_DOUT_BIT_REVERSE	R/W	0x0	GPIO8
		[30:0]	GPO8_DOUT_CFG		0x7E	
GPO8_DOEN_CFG	0x94	[31]	GPO8_DOEN_BIT_REVERSE	R/W	0x0	GPIO8
		[30:0]	GPO8_DOEN_CFG		0x0	
GPO9_DOUT_CFG	0x98	[31]	GPO9_DOUT_BIT_REVERSE	R/W	0x0	GPIO9
		[30:0]	GPO9_DOUT_CFG		0x0	
GPO9_DOEN_CFG	0x9C	[31]	GPO9_DOEN_BIT_REVERSE	R/W	0x0	GPIO9
		[30:0]	GPO9_DOEN_CFG		0x1	
GPO10_DOUT_CFG	0xA0	[31]	GPO10_DOUT_BIT_REVERSE	R/W	0x0	GPIO10
		[30:0]	GPO10_DOUT_CFG		0x0	
GPO10_DOEN_CFG	0xA4	[31]	GPO10_DOEN_BIT_REVERSE	R/W	0x0	GPIO10
		[30:0]	GPO10_DOEN_CFG		0x1	
GPO11_DOUT_CFG	0xA8	[31]	GPO11_DOUT_BIT_REVERSE	R/W	0x0	GPIO11
		[30:0]	GPO11_DOUT_CFG		0x0	
GPO11_DOEN_CFG	0xAC	[31]	GPO11_DOEN_BIT_REVERSE	R/W	0x0	GPIO11
		[30:0]	GPO11_DOEN_CFG		0x1	
GPO12_DOUT_CFG	0xB0	[31]	GPO12_DOUT_BIT_REVERSE	R/W	0x0	GPIO12

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO12_DOUT_CFG		0x7D	
GPO12_DOEN_CFG	0xB4	[31]	GPO12_DOEN_BIT_REVERSE	R/W	0x0	GPIO12
		[30:0]	GPO12_DOEN_CFG		0x0	
GPO13_DOUT_CFG	0xB8	[31]	GPO13_DOUT_BIT_REVERSE	R/W	0x0	GPIO13
		[30:0]	GPO13_DOUT_CFG		0x0	
GPO13_DOEN_CFG	0xBC	[31]	GPO13_DOEN_BIT_REVERSE	R/W	0x0	GPIO13
		[30:0]	GPO13_DOEN_CFG		0x1	
GPO14_DOUT_CFG	0xC0	[31]	GPO14_DOUT_BIT_REVERSE	R/W	0x0	GPIO14
		[30:0]	GPO14_DOUT_CFG		0x84	
GPO14_DOEN_CFG	0xC4	[31]	GPO14_DOEN_BIT_REVERSE	R/W	0x0	GPIO14
		[30:0]	GPO14_DOEN_CFG		0x0	
GPO15_DOUT_CFG	0xC8	[31]	GPO15_DOUT_BIT_REVERSE	R/W	0x0	GPIO15
		[30:0]	GPO15_DOUT_CFG		0x2F	
GPO15_DOEN_CFG	0xCC	[31]	GPO15_DOEN_BIT_REVERSE	R/W	0x0	GPIO15
		[30:0]	GPO15_DOEN_CFG		0x0	
GPO16_DOUT_CFG	0xD0	[31]	GPO16_DOUT_BIT_REVERSE	R/W	0x0	GPIO16
		[30:0]	GPO16_DOUT_CFG		0x30	
GPO16_DOEN_CFG	0xD4	[31]	GPO16_DOEN_BIT_REVERSE	R/W	0x0	GPIO16
		[30:0]	GPO16_DOEN_CFG		0x0	
GPO17_DOUT_CFG	0xD8	[31]	GPO17_DOUT_BIT_REVERSE	R/W	0x0	GPIO17
		[30:0]	GPO17_DOUT_CFG		0x31	
GPO17_DOEN_CFG	0xDC	[31]	GPO17_DOEN_BIT_REVERSE	R/W	0x0	GPIO17
		[30:0]	GPO17_DOEN_CFG		0x0	
GPO18_DOUT_CFG	0xE0	[31]	GPO18_DOUT_BIT_REVERSE	R/W	0x0	GPIO18
		[30:0]	GPO18_DOUT_CFG		0x0	
GPO18_DOEN_CFG	0xE4	[31]	GPO18_DOEN_BIT_REVERSE	R/W	0x0	GPIO18
		[30:0]	GPO18_DOEN_CFG		0x1	
GPO19_DOUT_CFG	0xE8	[31]	GPO19_DOUT_BIT_REVERSE	R/W	0x0	GPIO19

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO19_DOUT_CFG		0x0	
GPO19_DOEN_CFG	0xEC	[31]	GPO19_DOEN_BIT_REVERSE	R/W	0x0	GPIO19
		[30:0]	GPO19_DOEN_CFG		0x1	
GPO20_DOUT_CFG	0xF0	[31]	GPO20_DOUT_BIT_REVERSE	R/W	0x0	GPIO20
		[30:0]	GPO20_DOUT_CFG		0x0	
GPO20_DOEN_CFG	0xF4	[31]	GPO20_DOEN_BIT_REVERSE	R/W	0x0	GPIO20
		[30:0]	GPO20_DOEN_CFG		0x1	
GPO21_DOUT_CFG	0xF8	[31]	GPO21_DOUT_BIT_REVERSE	R/W	0x0	GPIO21
		[30:0]	GPO21_DOUT_CFG		0x0	
GPO21_DOEN_CFG	0xFC	[31]	GPO21_DOEN_BIT_REVERSE	R/W	0x0	GPIO21
		[30:0]	GPO21_DOEN_CFG		0x1	
GPO22_DOUT_CFG	0x100	[31]	GPO22_DOUT_BIT_REVERSE	R/W	0x0	GPIO22
		[30:0]	GPO22_DOUT_CFG		0x0	
GPO22_DOEN_CFG	0x104	[31]	GPO22_DOEN_BIT_REVERSE	R/W	0x0	GPIO22
		[30:0]	GPO22_DOEN_CFG		0x1	
GPO23_DOUT_CFG	0x108	[31]	GPO23_DOUT_BIT_REVERSE	R/W	0x0	GPIO23
		[30:0]	GPO23_DOUT_CFG		0x0	
GPO23_DOEN_CFG	0x10C	[31]	GPO23_DOEN_BIT_REVERSE	R/W	0x0	GPIO23
		[30:0]	GPO23_DOEN_CFG		0x1	
GPO24_DOUT_CFG	0x110	[31]	GPO24_DOUT_BIT_REVERSE	R/W	0x0	GPIO24
		[30:0]	GPO24_DOUT_CFG		0x0	
GPO24_DOEN_CFG	0x114	[31]	GPO24_DOEN_BIT_REVERSE	R/W	0x0	GPIO24
		[30:0]	GPO24_DOEN_CFG		0x1	
GPO25_DOUT_CFG	0x118	[31]	GPO25_DOUT_BIT_REVERSE	R/W	0x0	GPIO25
		[30:0]	GPO25_DOUT_CFG		0x0	
GPO25_DOEN_CFG	0x11C	[31]	GPO25_DOEN_BIT_REVERSE	R/W	0x0	GPIO25
		[30:0]	GPO25_DOEN_CFG		0x1	
GPO26_DOUT_CFG	0x120	[31]	GPO26_DOUT_BIT_REVERSE	R/W	0x0	GPIO26

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO26_DOUT_CFG		0x0	
GPO26_DOEN_CFG	0x124	[31]	GPO26_DOEN_BIT_REVERSE	R/W	0x0	GPIO26
		[30:0]	GPO26_DOEN_CFG		0x1	
GPO27_DOUT_CFG	0x128	[31]	GPO27_DOUT_BIT_REVERSE	R/W	0x0	GPIO27
		[30:0]	GPO27_DOUT_CFG		0x0	
GPO27_DOEN_CFG	0x12C	[31]	GPO27_DOEN_BIT_REVERSE	R/W	0x0	GPIO27
		[30:0]	GPO27_DOEN_CFG		0x1	
GPO28_DOUT_CFG	0x130	[31]	GPO28_DOUT_BIT_REVERSE	R/W	0x0	GPIO28
		[30:0]	GPO28_DOUT_CFG		0x0	
GPO28_DOEN_CFG	0x134	[31]	GPO28_DOEN_BIT_REVERSE	R/W	0x0	GPIO28
		[30:0]	GPO28_DOEN_CFG		0x1	
GPO29_DOUT_CFG	0x138	[31]	GPO29_DOUT_BIT_REVERSE	R/W	0x0	GPIO29
		[30:0]	GPO29_DOUT_CFG		0x0	
GPO29_DOEN_CFG	0x13C	[31]	GPO29_DOEN_BIT_REVERSE	R/W	0x0	GPIO29
		[30:0]	GPO29_DOEN_CFG		0x1	
GPO30_DOUT_CFG	0x140	[31]	GPO30_DOUT_BIT_REVERSE	R/W	0x0	GPIO30
		[30:0]	GPO30_DOUT_CFG		0x0	
GPO30_DOEN_CFG	0x144	[31]	GPO30_DOEN_BIT_REVERSE	R/W	0x0	GPIO30
		[30:0]	GPO30_DOEN_CFG		0x1	
GPO31_DOUT_CFG	0x148	[31]	GPO31_DOUT_BIT_REVERSE	R/W	0x0	GPIO31
		[30:0]	GPO31_DOUT_CFG		0x74	
GPO31_DOEN_CFG	0x14C	[31]	GPO31_DOEN_BIT_REVERSE	R/W	0x0	GPIO31
		[30:0]	GPO31_DOEN_CFG		0x70	
GPO32_DOUT_CFG	0x150	[31]	GPO32_DOUT_BIT_REVERSE	R/W	0x0	GPIO32
		[30:0]	GPO32_DOUT_CFG		0x75	
GPO32_DOEN_CFG	0x154	[31]	GPO32_DOEN_BIT_REVERSE	R/W	0x0	GPIO32
		[30:0]	GPO32_DOEN_CFG		0x71	
GPO33_DOUT_CFG	0x158	[31]	GPO33_DOUT_BIT_REVERSE	R/W	0x0	GPIO33

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO33_DOUT_CFG		0x76	
GPO33_DOEN_CFG	0x15C	[31]	GPO33_DOEN_BIT_REVERSE	R/W	0x0	GPIO33
		[30:0]	GPO33_DOEN_CFG		0x72	
GPO34_DOUT_CFG	0x160	[31]	GPO34_DOUT_BIT_REVERSE	R/W	0x0	GPIO34
		[30:0]	GPO34_DOUT_CFG		0x77	
GPO34_DOEN_CFG	0x164	[31]	GPO34_DOEN_BIT_REVERSE	R/W	0x0	GPIO34
		[30:0]	GPO34_DOEN_CFG		0x73	
GPO35_DOUT_CFG	0x168	[31]	GPO35_DOUT_BIT_REVERSE	R/W	0x0	GPIO35
		[30:0]	GPO35_DOUT_CFG		0x0	
GPO35_DOEN_CFG	0x16C	[31]	GPO35_DOEN_BIT_REVERSE	R/W	0x0	GPIO35
		[30:0]	GPO35_DOEN_CFG		0x1	
GPO36_DOUT_CFG	0x170	[31]	GPO36_DOUT_BIT_REVERSE	R/W	0x0	GPIO36
		[30:0]	GPO36_DOUT_CFG		0x0	
GPO36_DOEN_CFG	0x174	[31]	GPO36_DOEN_BIT_REVERSE	R/W	0x0	GPIO36
		[30:0]	GPO36_DOEN_CFG		0x1	
GPO37_DOUT_CFG	0x178	[31]	GPO37_DOUT_BIT_REVERSE	R/W	0x0	GPIO37
		[30:0]	GPO37_DOUT_CFG		0x0	
GPO37_DOEN_CFG	0x17C	[31]	GPO37_DOEN_BIT_REVERSE	R/W	0x0	GPIO37
		[30:0]	GPO37_DOEN_CFG		0x1	
GPO38_DOUT_CFG	0x180	[31]	GPO38_DOUT_BIT_REVERSE	R/W	0x0	GPIO38
		[30:0]	GPO38_DOUT_CFG		0x0	
GPO38_DOEN_CFG	0x184	[31]	GPO38_DOEN_BIT_REVERSE	R/W	0x0	GPIO38
		[30:0]	GPO38_DOEN_CFG		0x1	
GPO39_DOUT_CFG	0x188	[31]	GPO39_DOUT_BIT_REVERSE	R/W	0x0	GPIO39
		[30:0]	GPO39_DOUT_CFG		0x0	
GPO39_DOEN_CFG	0x18C	[31]	GPO39_DOEN_BIT_REVERSE	R/W	0x0	GPIO39
		[30:0]	GPO39_DOEN_CFG		0x1	
GPO40_DOUT_CFG	0x190	[31]	GPO40_DOUT_BIT_REVERSE	R/W	0x0	GPIO40

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO40_DOUT_CFG		0x0	
GPO40_DOEN_CFG	0x194	[31]	GPO40_DOEN_BIT_REVERSE	R/W	0x0	GPIO40
		[30:0]	GPO40_DOEN_CFG		0x1	
GPO41_DOUT_CFG	0x190	[31]	GPO41_DOUT_BIT_REVERSE	R/W	0x0	GPIO41
		[30:0]	GPO41_DOUT_CFG		0x0	
GPO41_DOEN_CFG	0x194	[31]	GPO41_DOEN_BIT_REVERSE	R/W	0x0	GPIO41
		[30:0]	GPO41_DOEN_CFG		0x1	
GPO42_DOUT_CFG	0x190	[31]	GPO42_DOUT_BIT_REVERSE	R/W	0x0	GPIO42
		[30:0]	GPO42_DOUT_CFG		0x0	
GPO42_DOEN_CFG	0x194	[31]	GPO42_DOEN_BIT_REVERSE	R/W	0x0	GPIO42
		[30:0]	GPO42_DOEN_CFG		0x1	
GPO43_DOUT_CFG	0x190	[31]	GPO43_DOUT_BIT_REVERSE	R/W	0x0	GPIO43
		[30:0]	GPO43_DOUT_CFG		0x0	
GPO43_DOEN_CFG	0x194	[31]	GPO43_DOEN_BIT_REVERSE	R/W	0x0	GPIO43
		[30:0]	GPO43_DOEN_CFG		0x1	
GPO44_DOUT_CFG	0x190	[31]	GPO44_DOUT_BIT_REVERSE	R/W	0x0	GPIO44
		[30:0]	GPO44_DOUT_CFG		0x0	
GPO44_DOEN_CFG	0x194	[31]	GPO44_DOEN_BIT_REVERSE	R/W	0x0	GPIO44
		[30:0]	GPO44_DOEN_CFG		0x1	
GPO45_DOUT_CFG	0x190	[31]	GPO45_DOUT_BIT_REVERSE	R/W	0x0	GPIO45
		[30:0]	GPO45_DOUT_CFG		0x0	
GPO45_DOEN_CFG	0x194	[31]	GPO45_DOEN_BIT_REVERSE	R/W	0x0	GPIO45
		[30:0]	GPO45_DOEN_CFG		0x1	
GPO46_DOUT_CFG	0x190	[31]	GPO46_DOUT_BIT_REVERSE	R/W	0x0	GPIO46
		[30:0]	GPO46_DOUT_CFG		0x0	
GPO46_DOEN_CFG	0x194	[31]	GPO46_DOEN_BIT_REVERSE	R/W	0x0	GPIO46
		[30:0]	GPO46_DOEN_CFG		0x1	
GPO47_DOUT_CFG	0x190	[31]	GPO47_DOUT_BIT_REVERSE	R/W	0x0	GPIO47

Register Name	Offset Address	Bit	Field	Type	Reset	For GPIO
		[30:0]	GPO47_DOUT_CFG		0x0	
GPO47_DOEN_CFG	0x194	[31]	GPO47_DOEN_BIT_REVERSE	R/W	0x0	GPIO47
		[30:0]	GPO47_DOEN_CFG		0x1	
GPO48_DOUT_CFG	0x190	[31]	GPO48_DOUT_BIT_REVERSE	R/W	0x0	GPIO48
		[30:0]	GPO48_DOUT_CFG		0x0	
GPO48_DOEN_CFG	0x194	[31]	GPO48_DOEN_BIT_REVERSE	R/W	0x0	GPIO48
		[30:0]	GPO48_DOEN_CFG		0x1	
GPO49_DOUT_CFG	0x190	[31]	GPO49_DOUT_BIT_REVERSE	R/W	0x0	GPIO49
		[30:0]	GPO49_DOUT_CFG		0x0	
GPO49_DOEN_CFG	0x194	[31]	GPO49_DOEN_BIT_REVERSE	R/W	0x0	GPIO49
		[30:0]	GPO49_DOEN_CFG		0x1	

12.3. Registers for Configuring GPIOs as Inputs for IP Block Signals

There are 75 signals (listed in Table 11-3) inside the device which can get connected to any one of the 64 GPIO pads and as such get their input from outside the device. Any signal can be configured to get its input from any one of the GPIO pads. Additionally, any of the signals can be connected to a digital 1 or 0. As such the size of *input signal set* is effectively 66 (digital 0 + digital 1 + 64 GPIO pads) and the size of the *output signal set* is 75. Seventy-five configuration registers, one for each signal of the output signal set, are used for making the connections between the input and the output signal sets. These configuration registers are defined in individual tables in this section.

The first row of each table, defining a configuration register, lists the name of the register along with the name and a brief description of the internal signal with which it is associated. Storing a value, in the range of 0 – 65, in a specific configuration register makes the connection between the input signal set and that specific internal signal. The value to be stored for digital 0 is 0, digital 1 is 1, PAD_GPIO[0] is 2, PAD_GPIO[1] is 3, … and PAD_GPIO[63] is 65. For example for signal GPI_CPU_JTAG_TCK some of the values that can be stored in register GPI_CPU_JTAG_TCK_CFG for connecting to a specific signal from the input signal set are:

Table 12-19 Values Stored in Configuration Register for Signal Input Connection

Connecting to	Value stored in GPI_CPU_JTAG_TCK_CFG	
	Hex	Decimal
Digital 0	0x0	0
Digital 1	0x1	1
GPIO[20]	0x16	22
GPIO[6]	0x8	8

A configuration register with a default value on power-up reset results in a default connection between a specific signal from the input signal set and that internal signal. Note that the connection can be changed after power-up by storing a different value in the register. The configuration registers are given in the following tables.

Table 12-20 GPI_CPU_JTAG_TCK_CFG

GPI_CPU_JTAG_TCK_CFG: Configuration Register for Signal GPI_CPU_JTAG_TCK (CPU JTAG Clock)			
Register Offset			0x250
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x3	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. On power-up reset the signal by default is connected to GPIO1 pad.

Table 12-21 GPI_CPU_JTAG_TDI_CFG

GPI_CPU_JTAG_TDI_CFG: Configuration Register for Signal GPI_CPU_JTAG_TDI (CPU JTAG Test Data In)			
Register Offset			0x254
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x4	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x4 (connected to GPIO2 pad.)

Table 12-22 GPI_CPU_JTAG_TMS_CFG

GPI_CPU_JTAG_TMS_CFG: Configuration Register for Signal GPI_CPU_JTAG_TMS (CPU JTAG Test Mode Select)			
Register Offset			0x258
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x5	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x5 (connected toGPIO3 pad.)

Table 12-23 GPI_CPU_JTAG_TRST_CFG

GPI_CPU_JTAG_TRST_CFG: Configuration Register for Signal GPI_CPU_JTAG_TRST (CPU JTAG Test Reset)			
Register Offset			0x25C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x6	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x6 (connected to GPIO4 pad.)

Table 12-24 Table 12-25GPI_DMIC_SDIN_BIT0_CFG

GPI_DMIC_SDIN_BIT0_CFG: Configuration Register for signal GPI_DMIC_SDIN_BIT0 (Serial Data In bit 0 for Digital Mic)			
Register Offset			0x260
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.

Table 12-26 GPI_DMIC_SDIN_BIT1_CFG

GPI_DMIC_SDIN_BIT1_CFG: Configuration Register for signal GPI_DMIC_SDIN_BIT0 (Serial Data In bit 1 for Digital Mic)			
Register Offset			0x264
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-27 GPI_DSP_JTCK_PAD_CFG

GPI_DSP_JTCK_PAD_CFG: Configuration Register for signal GPI_DSP_JTCK_PAD (DSP JTAG Clock)			
Register Offset			0x268
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x2F	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x2F (connected to GPIO45 pad.)

Table 12-28 GPI_DSP_JTDI_PAD_CFG

GPI_DSP_JTDI_PAD_CFG: Configuration Register for signal GPI_DSP_JTDI_PAD (DSP JTAG Test Data In)			
Register Offset			0x26C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x32	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x32 (connected to GPIO48 pad.)

Table 12-29 GPI_DSP_JTMS_PAD_CFG

GPI_DSP_JTMS_PAD_CFG: Configuration Register for signal GPI_DSP_JTMS_PAD (DSP JTAG Test Mode Select)			
Register Offset			0x270
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x30	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x30 (connected to GPIO46 pad.)

Table 12-30 GPI_DSP_TRST_PAD_CFG

GPI_DSP_TRST_PAD_CFG: Configuration Register for signal GPI_DSP_TRST_PAD (DSP JTAG Reset)			
Register Offset			0x274
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x2E	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x2E (connected to GPIO44 pad.)

Table 12-31 GPI_I2C0_PAD_SCK_IN_CFG

GPI_I2C0_PAD_SCK_IN_CFG: Configuration Register for signal GPI_I2C0_PAD_SCK_IN (I2C 0 Clock)			
Register Offset			0x278
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-32 GPI_I2C0_PAD_SDA_IN_CFG

GPI_I2C0_PAD_SDA_IN_CFG: Configuration Register for signal GPI_I2C0_PAD_SDA_IN (I2C 0 Data)			
Register Offset			0x27C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-33 GPI_I2C1_PAD_SCK_IN_CFG

GPI_I2C1_PAD_SCK_IN_CFG: Configuration Register for signal GPI_I2C1_PAD_SCK_IN (I2C 1 Clock)			
Register Offset			0x280
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-34 GPI_I2C1_PAD_SDA_IN_CFG

GPI_I2C1_PAD_SDA_IN_CFG: Configuration Register for signal GPI_I2C1_PAD_SDA_IN (I2C 1 Data)			
Register Offset			0x284
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-35 GPI_I2C2_PAD_SCK_IN_CFG

GPI_I2C2_PAD_SCK_IN_CFG: Configuration Register for signal GPI_I2C2_PAD_SCK_IN (I2C 2 Clock)			
Register Offset			0x288
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-36 GPI_I2C2_PAD_SDA_IN_CFG

GPI_I2C2_PAD_SDA_IN_CFG: Configuration Register for signal GPI_I2C2_PAD_SDA_IN (I2C 2 Data)			
Register Offset			0x28C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-37 GPI_I2C3_PAD_SCK_IN_CFG

GPI_I2C3_PAD_SCK_IN_CFG: Configuration Register for signal GPI_I2C3_PAD_SCK_IN (I2C 3 Clock)			
Register Offset			0x290
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-38 GPI_I2C3_PAD_SDA_IN_CFG

GPI_I2C3_PAD_SDA_IN_CFG: Configuration Register for signal GPI_I2C3_PAD_SDA_IN (I2C 3 Data)			
Register Offset			0x294
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-39 GPI_I2SRX_BCLK_IN_CFG

GPI_I2SRX_BCLK_IN_CFG: Configuration Register for signal GPI_I2SRX_BCLK_IN			
Register Offset			0x298
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-40 GPI_I2SRX_LRCK_IN_CFG

GPI_I2SRX_LRCK_IN_CFG: Configuration Register for signal GPI_I2SRX_LRCK_IN			
Register Offset			0x29C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-41 GPI_I2SRX_SDIN_BIT0_CFG

GPI_I2SRX_SDIN_BIT0_CFG: Configuration Register for signal GPI_I2SRX_SDIN_BIT0			
Register Offset			0x2A0
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-42 GPI_I2SRX_SDIN_BIT1_CFG

GPI_I2SRX_SDIN_BIT1_CFG: Configuration Register for signal GPI_I2SRX_SDIN_BIT1			
Register Offset			0x2A4
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-43 GPI_I2SRX_SDIN_BIT2_CFG

GPI_I2SRX_SDIN_BIT2_CFG: Configuration Register for signal GPI_I2SRX_SDIN_BIT2			
Register Offset			0x2A8
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-44 GPI_I2STX_BCLK_IN_CFG

GPI_I2STX_BCLK_IN_CFG: Configuration Register for signal GPI_I2STX_BCLK_IN			
Register Offset			0x2AC
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-45 GPI_I2STX_LRCK_IN_CFG

GPI_I2STX_LRCK_IN_CFG: Configuration Register for signal GPI_I2STX_LRCK_IN			
Register Offset			0x2B0
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-46 GPI_SDIO0_PAD_CARD_DETECT_N_CFG

GPI_SDIO0_PAD_CARD_DETECT_N_CFG: Configuration Register for signal GPI_SDIO0_PAD_CARD_DETECT_N (SDIO 0 Card Detect)			
Register Offset			0x2B4
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-47 GPI_SDIO0_PAD_CARD_WRITE_PRT_CFG

GPI_SDIO0_PAD_CARD_WRITE_PRT_CFG: Configuration Register for signal GPI_SDIO0_PAD_CARD_WRITE_PRT (SDIO 0 Card Write Protect)			
Register Offset			0x2B8
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-48 GPI_SDIO0_PAD_CCMD_IN_CFG

GPI_SDIO0_PAD_CCMD_IN_CFG: Configuration Register for signal GPI_SDIO0_PAD_CCMD_IN (SDIO 0 Command)			
Register Offset			0x2BC
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-49 GPI_SDIO0_PAD_CDATA_IN_BIT0_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT0_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT0 (SDIO 0 DATA In Bit 0)			
Register Offset			0x2C0
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-50 GPI_SDIO0_PAD_CDATA_IN_BIT1_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT1_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT1 (SDIO 0 DATA In Bit 1)			
Register Offset			0x2C4
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-51 GPI_SDIO0_PAD_CDATA_IN_BIT2_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT2_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT2 (SDIO 0 DATA In Bit 2)			
Register Offset			0x2C8
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-52 GPI_SDIO0_PAD_CDATA_IN_BIT3_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT3_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT3 (SDIO 0 DATA In Bit 3)			
Register Offset			0x2CC
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-53 GPI_SDIO0_PAD_CDATA_IN_BIT4_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT4_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT4 (SDIO 0 DATA In Bit 4)			
Register Offset			0x2D0
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-54 GPI_SDIO0_PAD_CDATA_IN_BIT5_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT5_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT5 (SDIO 0 DATA In Bit 5)			
Register Offset			0x2D4
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-55 GPI_SDIO0_PAD_CDATA_IN_BIT6_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT6_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT6 (SDIO 0 DATA In Bit 6)			
Register Offset			0x2D8
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-56 GPI_SDIO0_PAD_CDATA_IN_BIT7_CFG

GPI_SDIO0_PAD_CDATA_IN_BIT7_CFG: Configuration Register for signal GPI_SDIO0_PAD_CDATA_IN_BIT7 (SDIO 0 DATA In Bit 8)			
Register Offset			0x2DC
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-57 GPI_SDIO1_PAD_CARD_DETECT_N_CFG

GPI_SDIO1_PAD_CARD_DETECT_N_CFG: Configuration Register for signal GPI_SDIO1_PAD_CARD_DETECT_N (SDIO 1 Card Detect)			
Register Offset			0x2E0
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-58 GPI_SDIO1_PAD_CARD_WRITE_PRT_CFG

GPI_SDIO1_PAD_CARD_WRITE_PRT_CFG: Configuration Register for signal GPI_SDIO1_PAD_CARD_WRITE_PRT (SDIO 1 Card Write Protect)			
Register Offset			0x2E4
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-59 GPI_SDIO1_PAD_CCMD_IN_CFG

GPI_SDIO1_PAD_CCMD_IN_CFG: Configuration Register for signal GPI_SDIO1_PAD_CCMD_IN (SDIO 1 Command)			
Register Offset			0x2E8
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-60 GPI_SDIO1_PAD_CDATA_IN_BIT0_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT0_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT0 (SDIO 1 DATA In Bit 0)			
Register Offset			0x2EC
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-61 GPI_SDIO1_PAD_CDATA_IN_BIT1_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT1_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT1 (SDIO 1 DATA In Bit 1)			
Register Offset			0x2F0
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-62 GPI_SDIO1_PAD_CDATA_IN_BIT2_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT2_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT2 (SDIO 1 DATA In Bit 2)			
Register Offset			0x2F4
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-63 GPI_SDIO1_PAD_CDATA_IN_BIT3_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT3_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT3 (SDIO 1 DATA In Bit 3)			
Register Offset			0x2F8
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-64 GPI_SDIO1_PAD_CDATA_IN_BIT4_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT4_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT4 (SDIO 1 DATA In Bit 4)			
Register Offset			0x2FC
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-65 GPI_SDIO1_PAD_CDATA_IN_BIT5_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT5_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT5 (SDIO 1 DATA In Bit 5)			
Register Offset			0x300
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-66 GPI_SDIO1_PAD_CDATA_IN_BIT6_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT6_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT6 (SDIO 1 DATA In Bit 6)			
Register Offset			0x304
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-67 GPI_SDIO1_PAD_CDATA_IN_BIT7_CFG

GPI_SDIO1_PAD_CDATA_IN_BIT7_CFG: Configuration Register for signal GPI_SDIO1_PAD_CDATA_IN_BIT7 (SDIO 1 DATA In Bit 7)			
Register Offset			0x308
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-68 GPI_SPDIF_RX_SDIN_CFG

GPI_SPDIF_RX_SDIN_CFG: Configuration Register for signal GPI_SPDIF_RX_SDIN (S/PDIF Input Data)			
Register Offset			0x30C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-69 GPI_SPI0_PAD_RXD_CFG

GPI_SPI0_PAD_RXD_CFG: Configuration Register for signal GPI_SPI0_PAD_RXD (SPI 0 Input Data - MISO)			
Register Offset			0x310
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-70 GPI_SPI0_PAD_SS_IN_N_CFG

GPI_SPI0_PAD_SS_IN_N_CFG: Configuration Register for signal GPI_SPI0_PAD_SS_IN_N (SPI 0 Slave Select)			
Register Offset			0x314
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 1.)

Table 12-71 GPI_SPI1_PAD_RXD_CFG

GPI_SPI1_PAD_RXD_CFG: Configuration Register for signal GPI_SPI1_PAD_RXD (SPI 1 Input Data - MISO)			
Register Offset			0x318
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-72 GPI_SPI1_PAD_SS_IN_N_CFG

GPI_SPI1_PAD_SS_IN_N_CFG: Configuration Register for signal GPI_SPI1_PAD_SS_IN_N (SPI 1 Slave Select)			
Register Offset			0x31C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-73 GPI_SPI2_PAD_RXD_CFG

GPI_SPI2_PAD_RXD_CFG: Configuration Register for signal GPI_SPI2_PAD_RXD (SPI 2 Input Data - MISO)			
Register Offset			0x320
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-74 GPI_SPI2_PAD_SS_IN_N_CFG

GPI_SPI2_PAD_SS_IN_N_CFG: Configuration Register for signal GPI_SPI2_PAD_SS_IN_N (SPI 2 Slave Select)			
Register Offset			0x324
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-75 GPI_SPI2AHB_PAD_RXD_BIT0_CFG

GPI_SPI2AHB_PAD_RXD_BIT0_CFG: Configuration Register for signal GPI_SPI2AHB_PAD_RXD_BIT0 (SPI 2 to AHB Bridge Input Data Bit 0)			
Register Offset			0x328
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x21	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x21 (connected to GPIO31 pad.)

Table 12-76 GPI_SPI2AHB_PAD_RXD_BIT1_CFG

GPI_SPI2AHB_PAD_RXD_BIT1_CFG: Configuration Register for signal GPI_SPI2AHB_PAD_RXD_BIT1 (SPI 2 to AHB Bridge Input Data Bit 1)			
Register Offset			0x32C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x22	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x22 (connected to GPIO32 pad.)

Table 12-77 GPI_SPI2AHB_PAD_RXD_BIT2_CFG

GPI_SPI2AHB_PAD_RXD_BIT2_CFG: Configuration Register for signal GPI_SPI2AHB_PAD_RXD_BIT2 (SPI 2 to AHB Bridge Input Data Bit 2)			
Register Offset			0x330
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x23	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x23 (connected to GPIO33 pad.)

Table 12-78 GPI_SPI2AHB_PAD_RXD_BIT2_CFG

GPI_SPI2AHB_PAD_RXD_BIT3_CFG: Configuration Register for signal GPI_SPI2AHB_PAD_RXD_BIT3 (SPI 2 to AHB Bridge Input Data Bit 3)			
Register Offset			0x334
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x24	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x24 (connected to GPIO34 pad.)

Table 12-79 GPI_SPI2AHB_PAD_SS_N_CFG

GPI_SPI2AHB_PAD_SS_N_CFG: Configuration Register for signal GPI_SPI2AHB_PAD_SS_N (SPI 2 to AHB Bridge Slave Select)			
Register Offset			0x338
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1F	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1F (connected to GPIO29 pad.)

Table 12-80 GPI_SPI2AHB_SLV_SCLKIN_CFG

GPI_SPI2AHB_SLV_SCLKIN_CFG: Configuration Register for signal GPI_SPI2AHB_SLV_SCLKIN (SPI 2 to AHB Bridge Clock)			
Register Offset			0x33C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x20	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x20 (connected to GPIO30] pad.)

Table 12-81 GPI_SPI3_PAD_RXD_CFG

GPI_SPI3_PAD_RXD_CFG: Configuration Register for signal GPI_SPI3_PAD_RXD (SPI 3 Input Data - MISO)			
Register Offset			0x340
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-82 GPI_SPI3_PAD_SS_IN_N_CFG

GPI_SPI3_PAD_SS_IN_N_CFG: Configuration Register for signal GPI_SPI3_PAD_SS_IN_N (SPI 3 Slave Select)			
Register Offset			0x344
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-83 GPI_UART0_PAD_CTSN_CFG

GPI_UART0_PAD_CTSN_CFG: Configuration Register for signal GPI_UART0_PAD_CTSN (UART 0 CTS)			
Register Offset			0x348
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x9	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x9 (connected to GPIO7 pad.)

Table 12-84 GPI_UART0_PAD_DCDN_CFG

GPI_UART0_PAD_DCDN_CFG: Configuration Register for signal GPI_UART0_PAD_DCDN (UART 0 DCD)			
Register Offset			0x34C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0xB	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0xB (connected to GPIO9 pad.)

Table 12-85 GPI_UART0_PAD_DSRN_CFG

GPI_UART0_PAD_DSRN_CFG: Configuration Register for signal GPI_UART0_PAD_DSRN (UART 0 DSR)			
Register Offset			0x350
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0xD	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0xD (connected to GPIO11 pad.)

Table 12-86 GPI_UART0_PAD_RIN_CFG

GPI_UART0_PAD_RIN_CFG: Configuration Register for signal GPI_UART0_PAD_RIN (UART 0 RI)			
Register Offset			0x354
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0xC	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0xC (connected to GPIO10 pad.)

Table 12-87 GPI_UART0_PAD_SIN_CFG

GPI_UART0_PAD_SIN_CFG: Configuration Register for signal GPI_UART0_PAD_SIN (UART 0 Input Data)			
Register Offset			0x358
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x7	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x7 (connected to GPIO5 pad.)

Table 12-88 GPI_UART1_PAD_SIN_CFG

GPI_UART1_PAD_SIN_CFG: Configuration Register for signal GPI_UART1_PAD_SIN (UART 1 Input Data)			
Register Offset			0x35C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-89 GPI_UART2_PAD_CTS_N_CFG

GPI_UART2_PAD_CTS_N_CFG: Configuration Register for signal GPI_UART2_PAD_CTS_N (UART 2 CTS)			
Register Offset			0x360
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-90 GPI_UART2_PAD_DCD_N_CFG

GPI_UART2_PAD_DCD_N_CFG: Configuration Register for signal GPI_UART2_PAD_DCD_N (UART 2 DCD)			
Register Offset			0x364
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-91 GPI_UART2_PAD_DSR_N_CFG

GPI_UART2_PAD_DSR_N_CFG: Configuration Register for signal GPI_UART2_PAD_DSR_N (UART 2 DSR)			
Register Offset			0x368
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-92 GPI_UART2_PAD_RI_N_CFG

GPI_UART2_PAD_RI_N_CFG: Configuration Register for signal GPI_UART2_PAD_RI_N (UART 2 RI)			
Register Offset			0x36C
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

Table 12-93 GPI_UART2_PAD_SIN_CFG

GPI_UART2_PAD_SIN_CFG: Configuration Register for signal GPI_UART2_PAD_SIN (UART 2 Input Data)			
Register Offset			0x370
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x1	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x1 (connected to digital 1.)

Table 12-94 GPI_UART3_PAD_SIN_CFG

GPI_UART3_PAD_SIN_CFG: Configuration Register for signal GPI_UART3_PAD_SIN (UART 3 Input Data)			
Register Offset			0x374
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0xF	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0xF (connected to GPIO13 pad.)

Table 12-95 GPI_USB_OVER_CURRENT_CFG

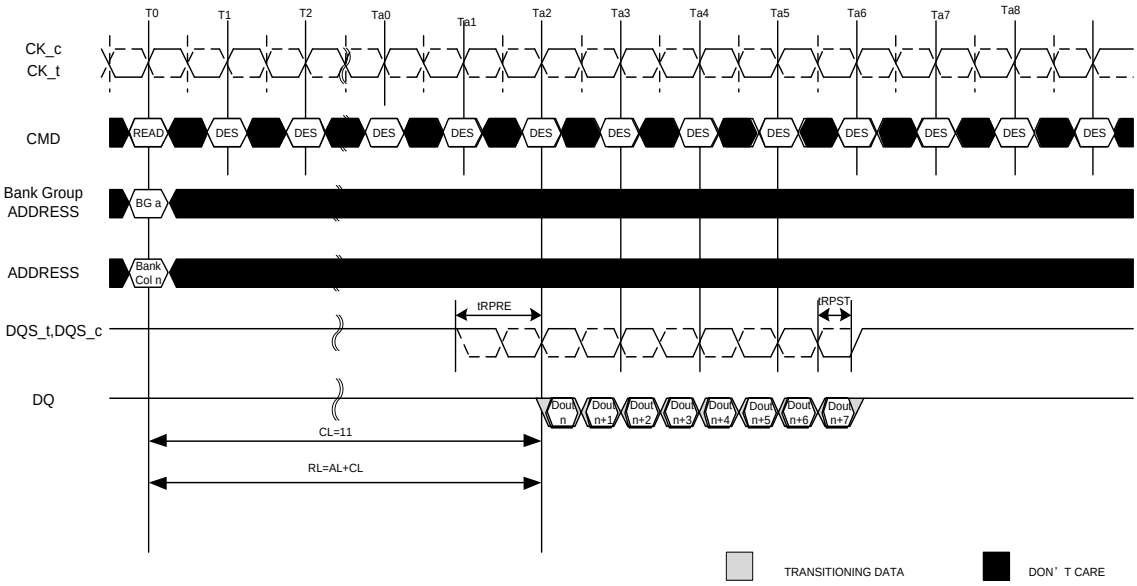
GPI_USB_OVER_CURRENT_CFG: Configuration Register for signal GPI_USB_OVER_CURRENT (USB Over Current Detect)			
Register Offset			0x378
Bit	**Type**	**Reset**	**Description**
[31:0]	R/W	0x0	Connects the signal to either a digital 0, digital 1 or any of the GPIO pads. [Default] 0x0 (connected to digital 0.)

13. Interface and AC Timing

13.1. DDR Interface and Timing

- **DDR4/DDR3:**

READ Burst Operation RL=11(AL=0, CL=11, BL8)



NOTE1 BL=8,AL=0,CL=11,Preamble=1tCK

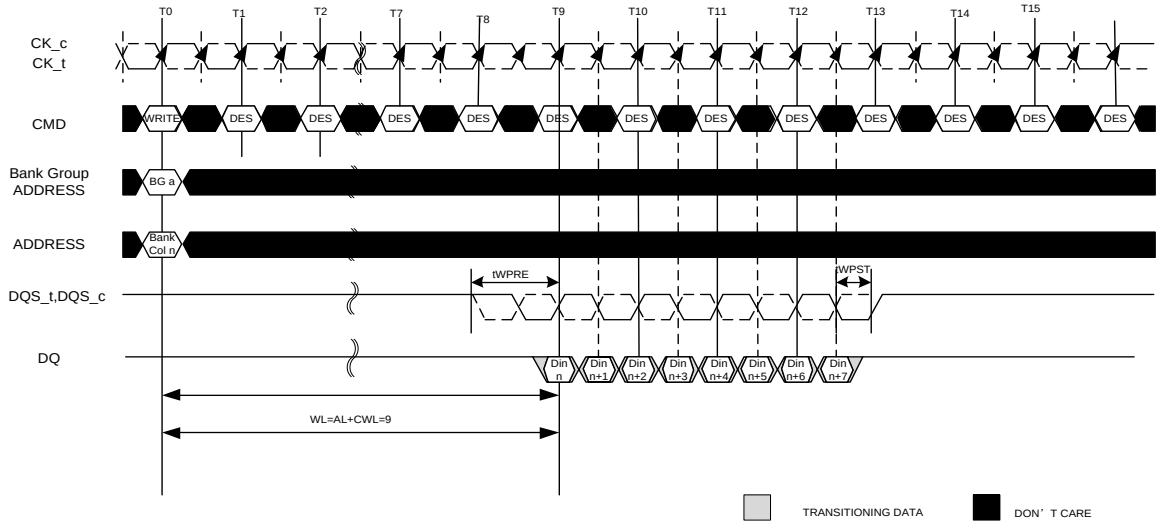
NOTE2 DOUTn=data-out from column n.

NOTE3 DES commands are shown for ease of illustration;other commands may be valid at these times.

NOTE4 BL8 setting activated by either MR0[A1:0=00]or MR0[A1:0=01]and A12=1 during READ command at T0.

Figure 13-1 DDR Read Burst Operation

WRITE Burst Operation WL=9(AL=0, CWL=9, BL8)

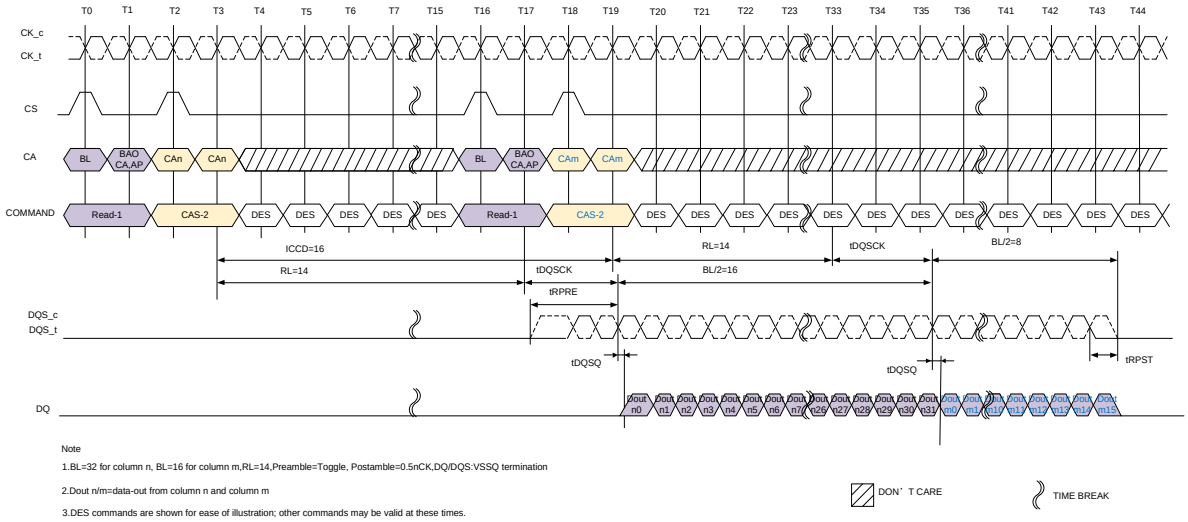


NOTE1 BL=8,WL=0,CWL=11,Preamble=1tCK
NOTE2 DOUTn=data-in to column n.
NOTE3 DES commands are shown for ease of illustration;other commands may be valid at these times.
NOTE4 BL8 setting activated by either MR0[A1:A0=00]or MR0[A1:A0=01]and A12=1 during WRITE command at T0.
NOTE5 CA Parity=Disable,CS to CA Latency = Disable, Write DBI= Disable .

Figure 13-2 DDR Write Burst Operation

- **LPDDR4:**

Burst Read



Note
1.BL=32 for column n, BL=16 for column m,RL=14,Preamble=Toggle, Postamble=0.5nCK,DQ/DQS:VSSQ termination
2.Dout n/m=data-out from column n and column m
3.DES commands are shown for ease of illustration; other commands may be valid at these times.

Figure 13-3 LPDDR4 Burst Read

Burst Write

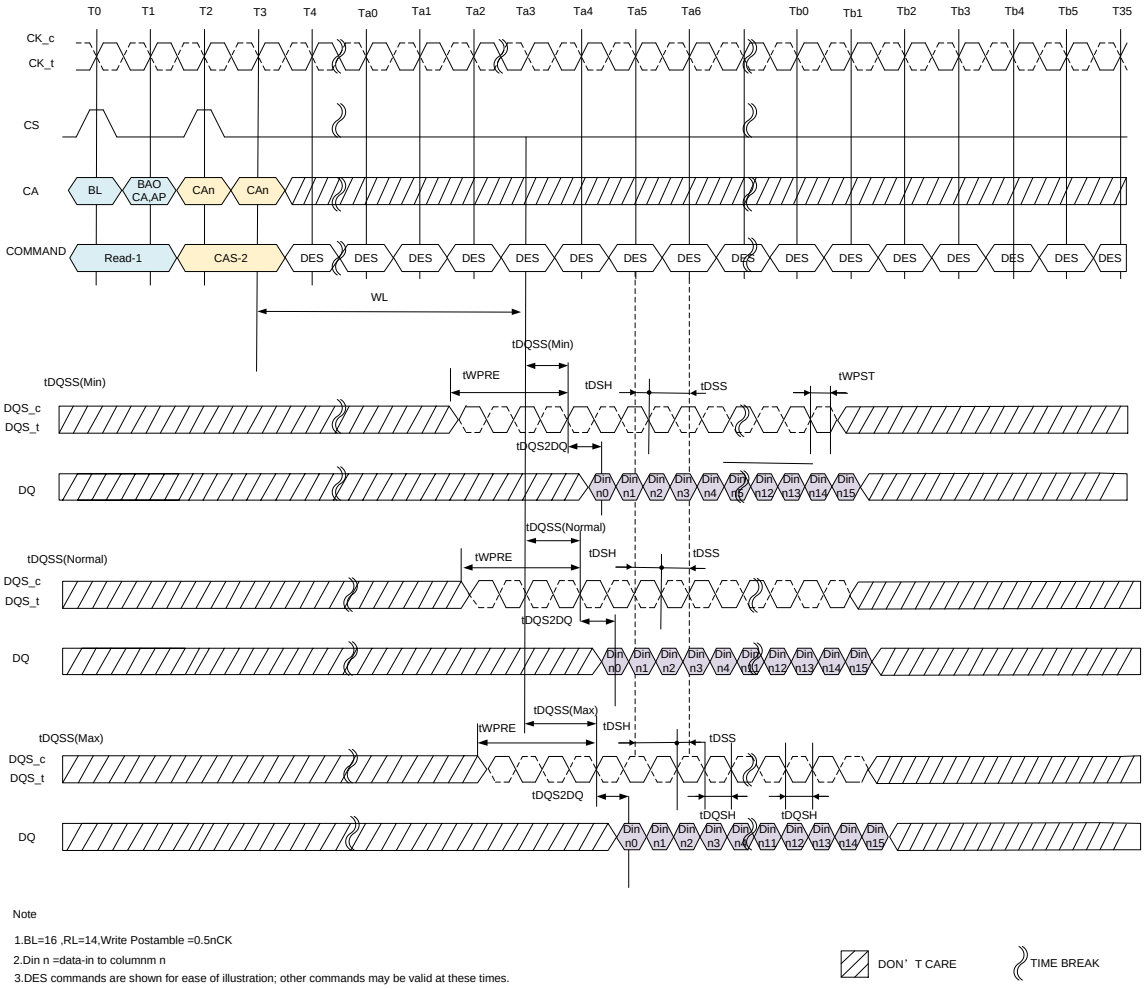


Figure 13-4 LPDDR4 Burst Write

- **LPDDR3:**

Burst Read: RL=12, BL=8, $t_{DQSCK} > t_{CK}$

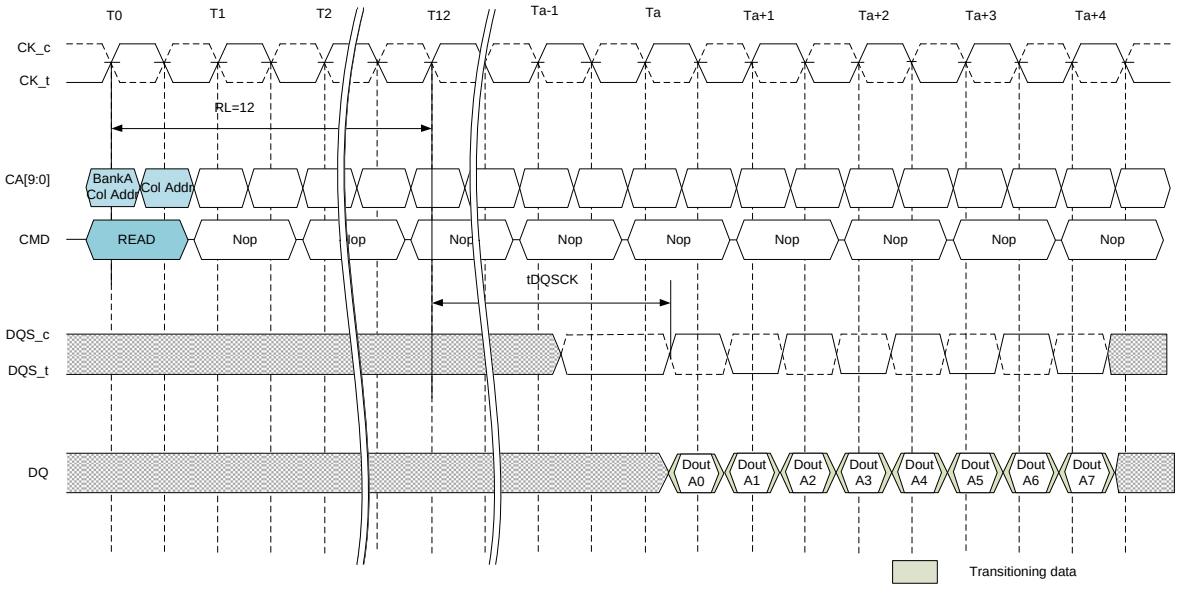


Figure 13-5 LPDDR3 Burst Read

Burst Write

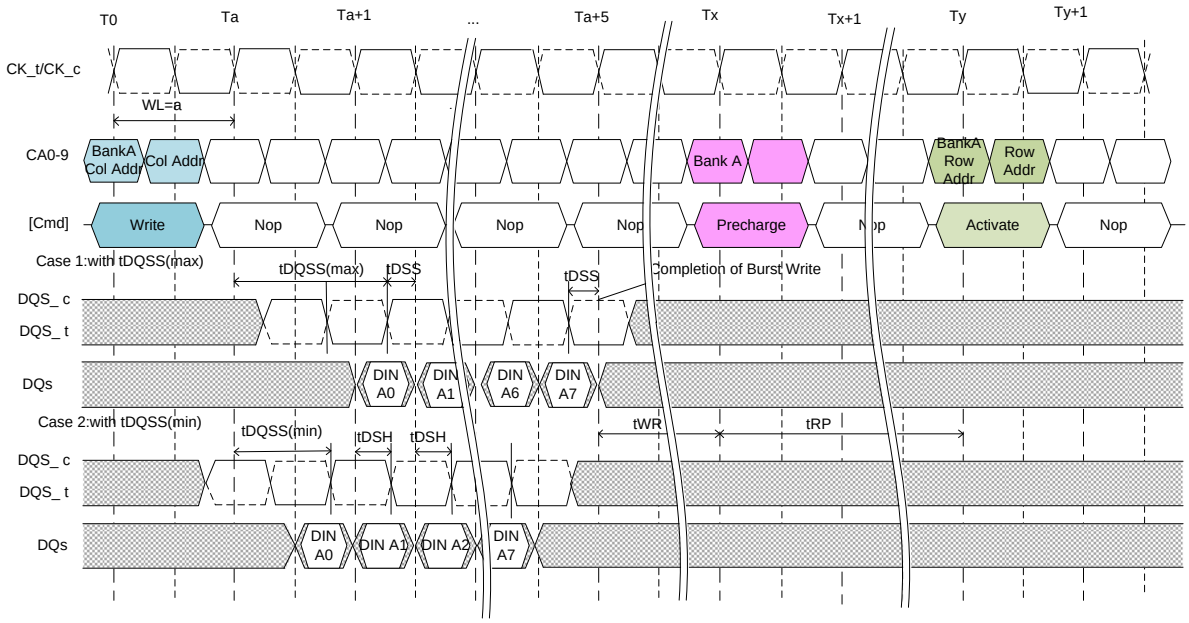


Figure 13-6 LPDDR3 Burst Write

13.2. RGMII Interface and Timing

RGMII Transmit

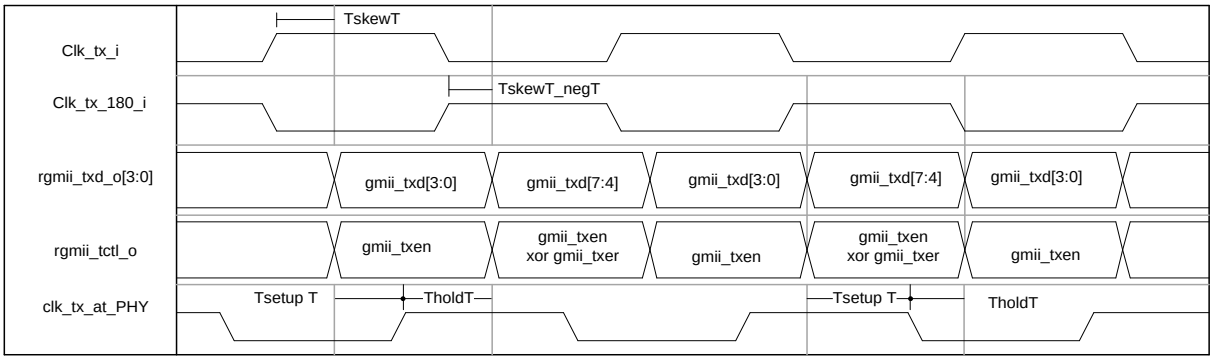


Figure 13-7 RGMII Transmit

RGMII Receive

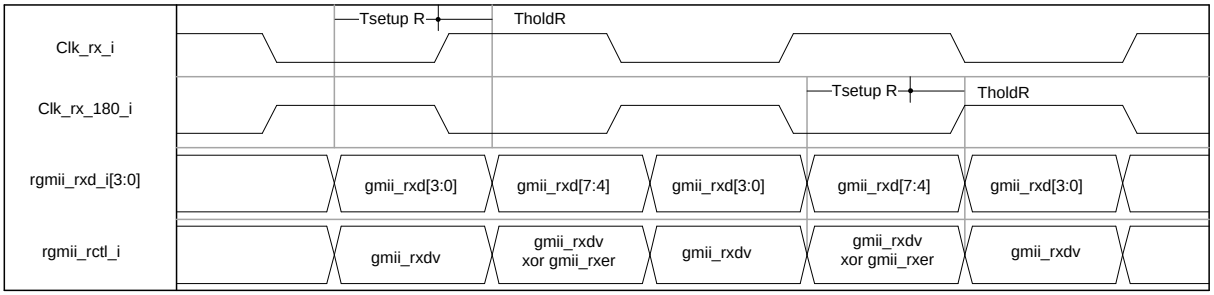


Figure 13-8 RGMII Receive

13.3. ChipLink Interface and Timing

ChipLink Tx

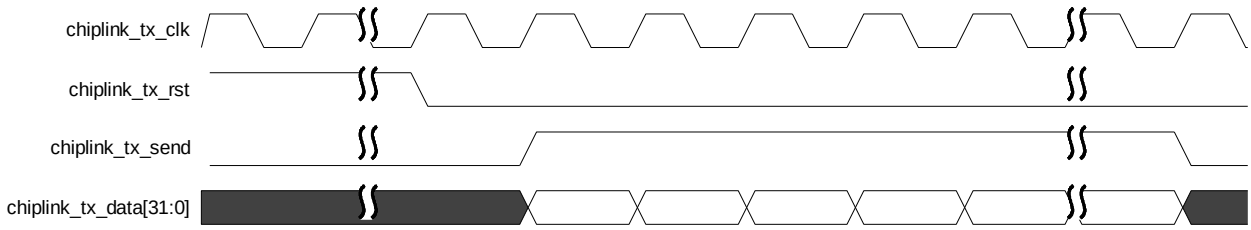


Figure 13-9 ChipLink TX

ChipLink Rx

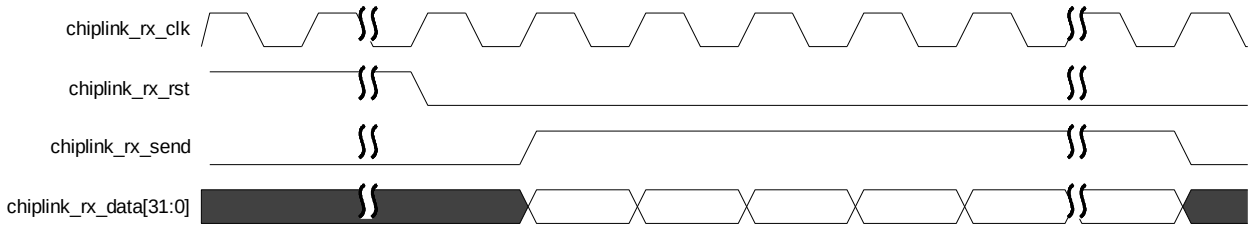


Figure 13-10 ChipLink RX

13.4. QSPI Interface and Timing

Quad Output Fast Read Array (6Bh/6Ch)

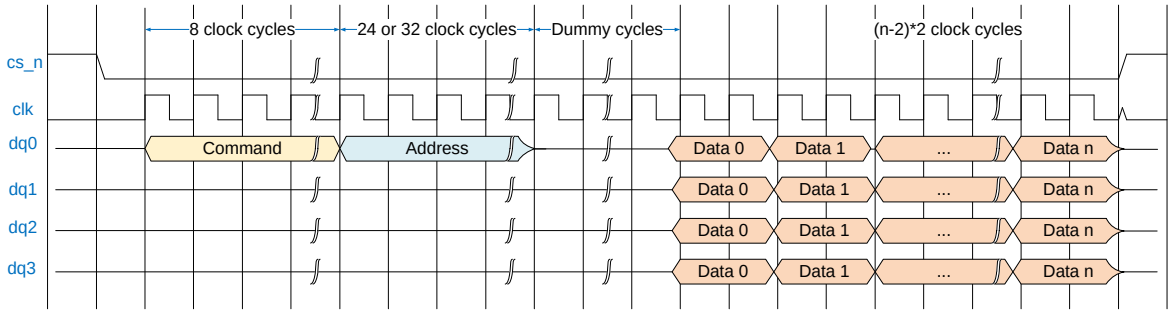


Figure 13-11 QSPI Fast read

Quad Input Fast Byte/Page Program (32h/34h)

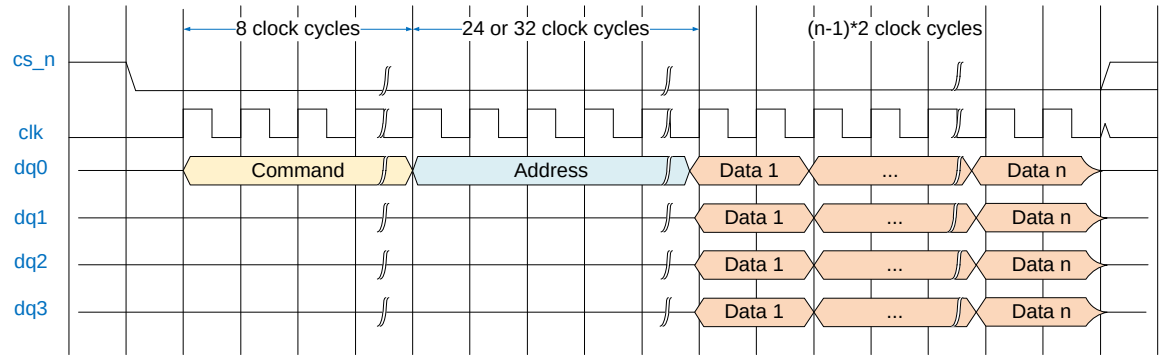


Figure 13-12 QSPI Fast Byte/Page Program

13.5. SPI Interface and Timing

SPI Read

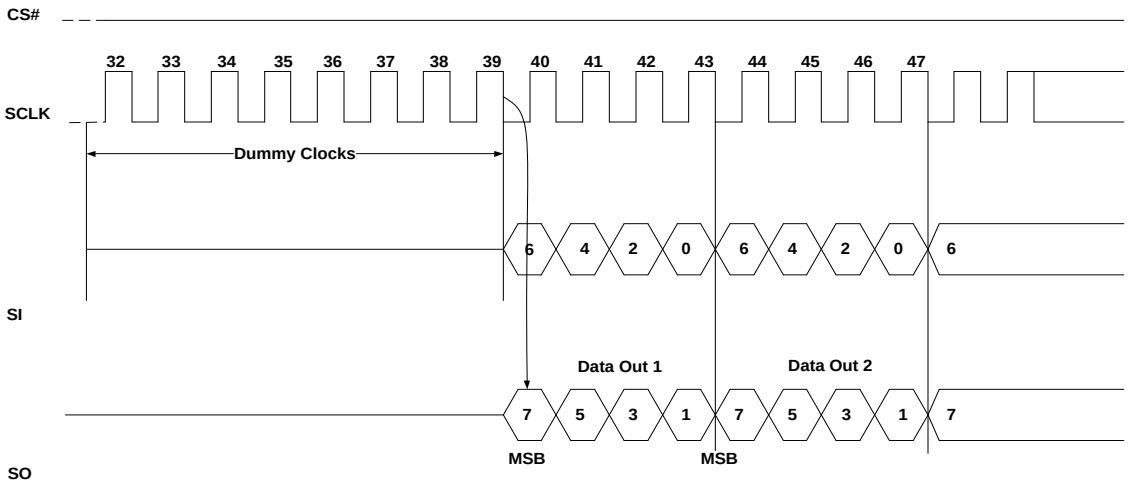


Figure 13-13 SPI Read

SPI Write

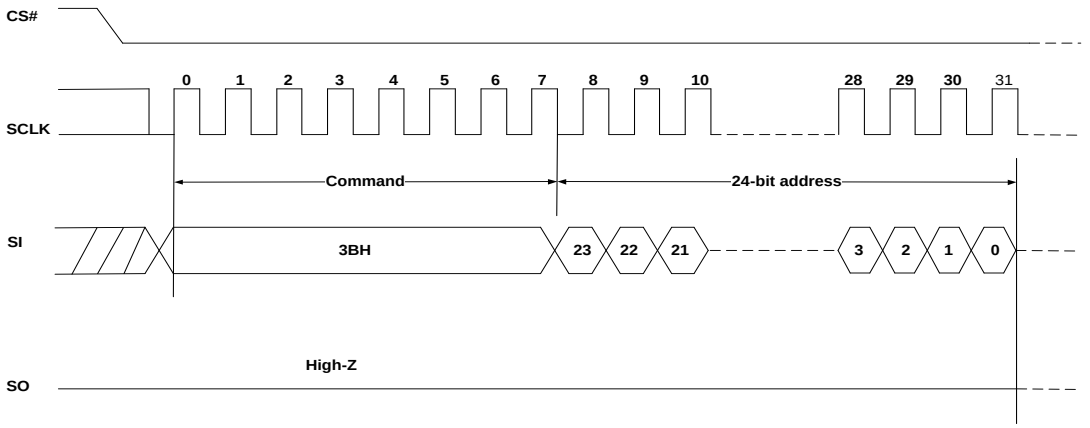


Figure 13-14 SPI Write

13.6. I2C Interface and Timing

Data transfer on the I2C Bus

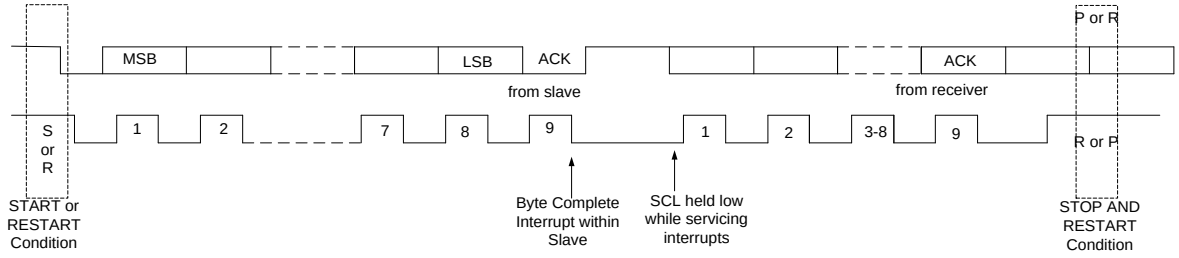


Figure 13-15 I2C Bus

14. Electrical Parameters

14.1. Absolute Maximum Ratings

Table 14-1 Absolute Maximum Ratings

Symbol	Parameters	Min	Max	Units
VDD	Power supply for Core	0.81	0.99	V
VDDIO	Power supply for Post-Driver	1.62	1.98	V
VDD3318	Power supply for 18OD33 IO Post-Driver	1.71	3.465	V
Vimax	Maximum Input Voltage	-	1.98	V
VDDramp-upslew	Ramp up slew for VDD	-	0.018	V/us
VDDIOramp-upslew	Ramp up slew for VDDIO	-	0.018	V/us
Tj	Junction Temperature	-40	125	℃
Ts	Storage temperature	0	70	℃

14.2. Recommended Operating Conditions

Table 14-2 Recommended Operating Conditions

Power	Ground	Description	Voltage			
			Min	Nom	Max	Units
VDD	VSS	Core power supply	0.81	0.9	0.99	V
VDD18		Digital IO power supply	1.62	1.8	1.98	V
VDD3318_CHIPLINK		FUNC_SHARE[0-69] IO power supply	3.135	3.3	3.465	V
VDD3318_LCD		FUNC_SHARE[70-97] IO power supply	3.135	3.3	3.465	V
VDD3318_SENSOR		FUNC_SHARE[98-114] IO power supply	3.135	3.3	3.465	V
VDD3318_GMII		FUNC_SHARE[115-141] IO power supply	3.135	3.3	3.465	V
AVDD18_MIPITX	VSS	MIPI TX analog power supply	1.62	1.8	1.98	V
AVDD18_MIPIRX	AVSS_MIPIRX	MIPI RX analog power supply for LDO	1.62	1.8	1.98	V
AVDD09_MIPIRX		MIPI RX analog power supply	0.855	0.9	0.99	V
AVDD18_TS	VSS18_TS	Temperature sensor analog power supply	1.62	1.8	1.98	V
AVDD33_USB	AVSS_USB	USB analog power supply	2.97	3.3	3.63	V
AVDD18_USB		USB analog power supply	1.62	1.8	1.98	V

Power		Ground	Description	Voltage			
				Min	Nom	Max	Units
AVDD09TX_USB		AVSSTX_USB	USB TX analog power supply	0.85	0.9	0.95	V
AVDD09RX_USB		AVSSRX_USB	USB RX analog power supply	0.85	0.9	0.95	V
DVDD18_OTP		VSS18_OTP	OTP power supply	1.62	1.8	1.98	V
AVDD09_PLL0		AVSS_PLL0	PLL0 analog power supply	0.81	0.9	0.99	V
AVDD09_PLL1		AVSS_PLL1	PLL1 analog power supply	0.81	0.9	0.99	V
AVDD09_PLL2		AVSS_PLL2	PLL2 analog power supply	0.81	0.9	0.99	V
DDR4/LPDDR4	VDDPLL_DDR0	VSS	DDR0 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR0		DDR0 IO power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDQCK_DDR0		DDR0 CK power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDPLL_DDR1		DDR1 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR1		DDR1 IO power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
	VDDQCK_DDR1		DDR1 CK power supply	1.14/1.06	1.2/1.1	1.26/1.17	V
DDR3/LPDDR3	VDDPLL_DDR0	VSS	DDR0 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR0		DDR0 IO power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDQCK_DDR0		DDR0 CK power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDPLL_DDR1		DDR1 PLL power supply	0.81	0.9	0.99	V
	VDDQ_DDR1		DDR1 IO power supply	1.425/1.14	1.5/1.2	1.575/1.3	V
	VDDQCK_DDR1		DDR1 CK power supply	1.425/1.14	1.5/1.2	1.575/1.3	V

14.3. DC Characteristics

Table 14-3 DC Characteristics (1.8 IO, VDDIO=1.8V)

Symbol	Parameters	Min	Nom	Max	Units
VIL	Input Low Voltage	-0.3	-	0.35*VDDIO	V
VIH	Input High Voltage	0.65*VDDIO	-	1.98	V
VT	Threshold Point	0.82	0.89	0.97	V
Ii	Input Leakage Current @Vi=1.8V or 0V	-	-	±10u	A
Ioz	Tri-state Output Leakage Current @Vi=1.8V or 0V	-	-	±10u	A
Rpu	Pull-up Resistor	60k	89k	137k	Ω
Rpd	Pull-down Resistor	61k	104k	196k	Ω

VOL	Output Low Voltage	-	-	0.45	V
VOH	Output High Voltage	1.35	-	-	V
IOL	Low Level Output Current @VOL(max)	16.5	27	37.7	mA
IOH	High Level Output Current @VOH(min)	19.5	28.5	39	mA

Table 14-4 DC Characteristics (18OD33 IO, VDD3318=3.3V)

Symbol	Parameters	Min	Nom	Max	Units
VIL	Input Low Voltage	-0.3	-	0.8	V
VIH	Input High Voltage	2.0	-	3.465	V
VT	Threshold Point	1.02	1.17	1.36	V
Ii	Input Leakage Current @Vi=3.3V or 0V	-	-	±10u	A
Ioz	Tri-state Output Leakage Current @Vi=3.3V or 0V	-	-	±10u	A
Rpu	Pull-up Resistor	26k	46k	71k	Ω
Rpd	Pull-down Resistor	27k	48k	103k	Ω
VOL	Output Low Voltage	-	-	0.4	V
VOH	Output High Voltage	2.4	-	-	V
IOL	Low Level Output Current @VOL(max)				
	DS2,DS1,DS0=000	4.0	6.3	8.9	mA
	DS2,DS1,DS0=001	6.0	9.4	13.3	mA
	DS2,DS1,DS0=010	8.0	12.5	17.6	mA
	DS2,DS1,DS0=011	9.9	15.5	21.8	mA
	DS2,DS1,DS0=100	11.9	18.6	26.1	mA
	DS2,DS1,DS0=101	13.9	21.6	30.2	mA
	DS2,DS1,DS0=110	15.8	24.5	34.2	mA
	DS2,DS1,DS0=111	17.7	27.4	38.1	mA
IOH	High Level Output Current @VOH(min)				
	DS2,DS1,DS0=000	5.9	9.3	14.2	mA
	DS2,DS1,DS0=001	8.8	13.9	21.2	mA
	DS2,DS1,DS0=010	11.7	18.5	28.2	mA
	DS2,DS1,DS0=011	14.6	23.1	35.2	mA
	DS2,DS1,DS0=100	17.5	27.7	42.2	mA
	DS2,DS1,DS0=101	20.3	32.2	49.1	mA
	DS2,DS1,DS0=110	23.2	36.8	56.0	mA
	DS2,DS1,DS0=111	26.1	41.3	62.8	mA

15. Supported Standards

15.1. LPDDR4/LPDDR3/DDR3/DDR4

- JESD209-3C
- JESD79-3D
- JESD79-4A
- JESD209-4B
- DFI 3.1 Specification
- Preliminary DFI 4.0 Specification Addendum to DFI 3.1

15.2. USB 2.0/3.0

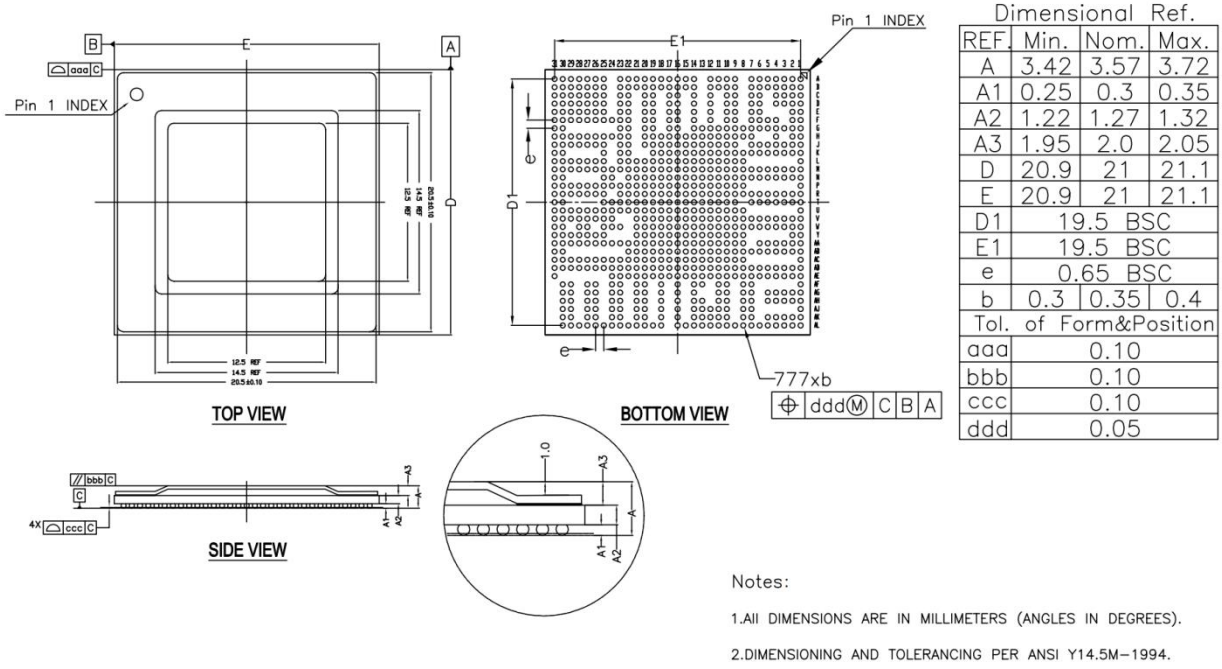
- USB-IF. On-The-Go and Embedded Host Supplement to USB Revision 2.0 Specification. July 27,2012. Revision 2.0 version 1.1a.
- USB-IF. On-The-Go and Embedded Host Supplement to the USB Revision 3.0 Specification. May 10,2012. Revision 1.1.
- Universal Serial Bus 3.0 Specification, Revision 1.0.
- PHY Interface For the PCI Express and USB 3.0 Architectures. 2009.
- Philips. UTMI+ Specification, Revision 1.0. 2004.

15.3. Ethernet Mac

- IEEE 802.3-2008 standard Gigabit Media Independent Interface (GMII)
- IEEE 1588-2008 standard for precision networked clock synchronization
- IEEE 802.3az-2010, for Energy Efficient Ethernet (EEE)
- RMII specification version 1.2 from RMII consortium

16. Package Specification

16.1. Package Outline



Dimensional Ref.

REF.	Min.	Nom.	Max.
A	3.42	3.57	3.72
A1	0.25	0.3	0.35
A2	1.22	1.27	1.32
A3	1.95	2.0	2.05
D	20.9	21	21.1
E	20.9	21	21.1
D1	19.5 BSC		
E1	19.5 BSC		
e	0.65 BSC		
b	0.3	0.35	0.4
Tol. of Form&Position			
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		

Figure 16-1 Package POD_FCBGA777