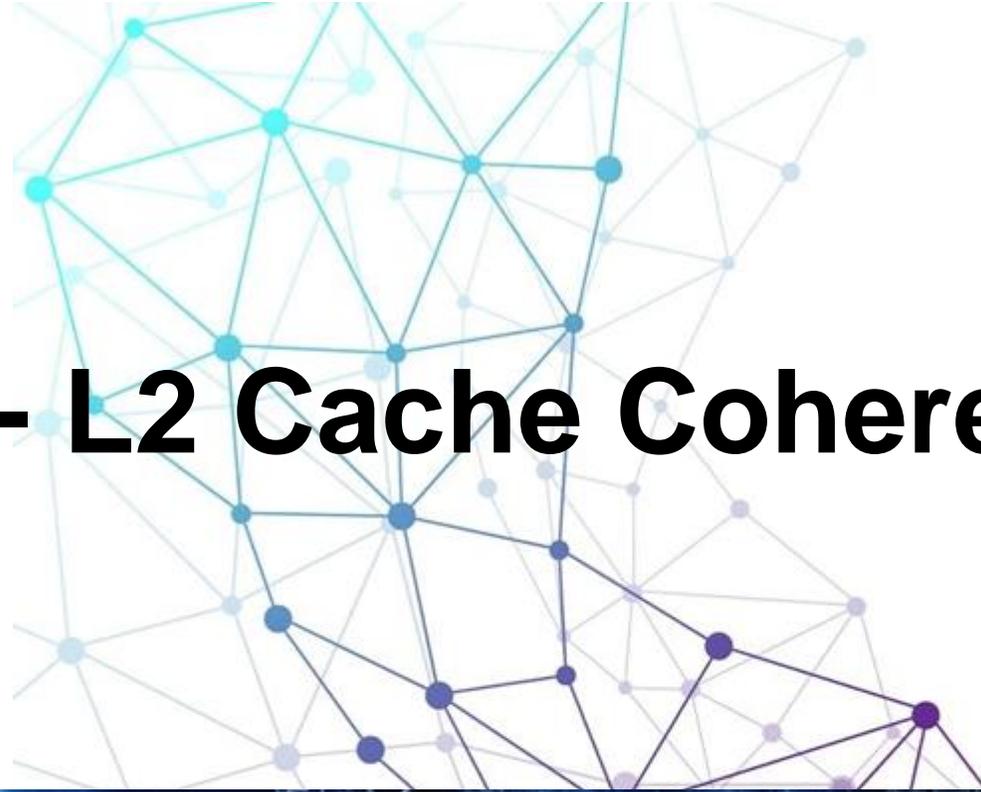


Memorandum - L2 Cache Coherence

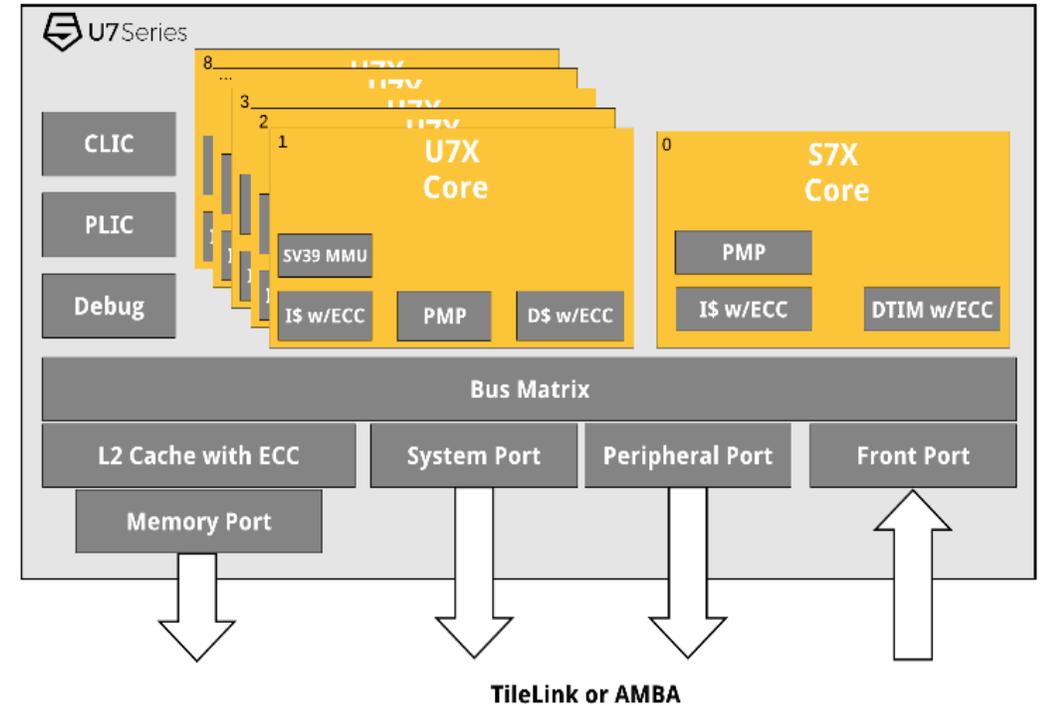




About U7 Series CPU core – used by JH71XX

U7 - High Performance 64-bit RISC-V Multi-Core Application Processor

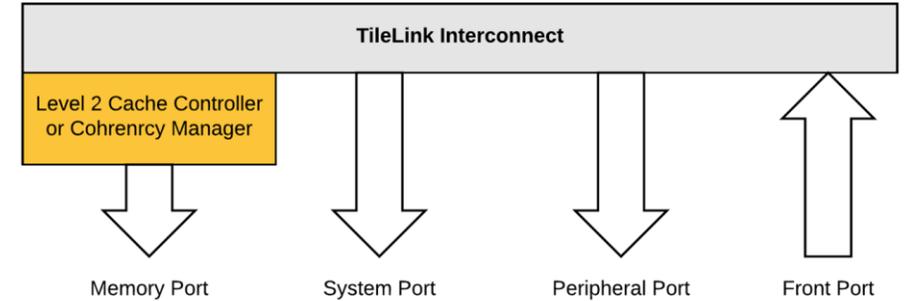
- U7 allows for instantiation of up to 9 U7 and/or S5 cores as well as a configurable Level 2 Cache
- U7 Core Architectural Features
 - RV64GCV capable core with Sv39/Sv48 Virtual Memory Support
 - Dual Issue, in-order 8 stage Harvard Pipeline
 - Optional SECDED ECC support on Level 1 and Level 2 memories
- Performance and Area
 - DMIPS – 2.5 DMIPS/MHz
 - Coremark – 5.1 Coremarks/MHz
 - SPEC – U54 + 40%
 - Core Area is ~30% larger than equivalent U5 Core
- Functional Safety and Security and Real Time features
 - SECDED ECC on all L1 and L2 memories
 - User Mode Interrupts for compartmentalization
 - Programmatically clear and/or disable dynamic branch prediction for deterministic execution and enhanced security
- Configurable EXX minion cores can provide a variety uses
 - System boot and monitor, Sensor Hub/Fusion, Security Co-Processor
- Broad market applications
 - General purpose embedded, industrial, IoT, high-performance real-time embedded, automotive





L2 Memory System for U7

- Inner TileLink Interconnect connects all Core Complex devices to the Level 2 Memory System
- All exposed ports can be independently configured to support your desired protocol
 - TileLink, AXI4, AHB-Lite, APB
- Memory, Front, and Peripheral Ports have configurable data bus widths
 - 32bit, 64bit, 128bit

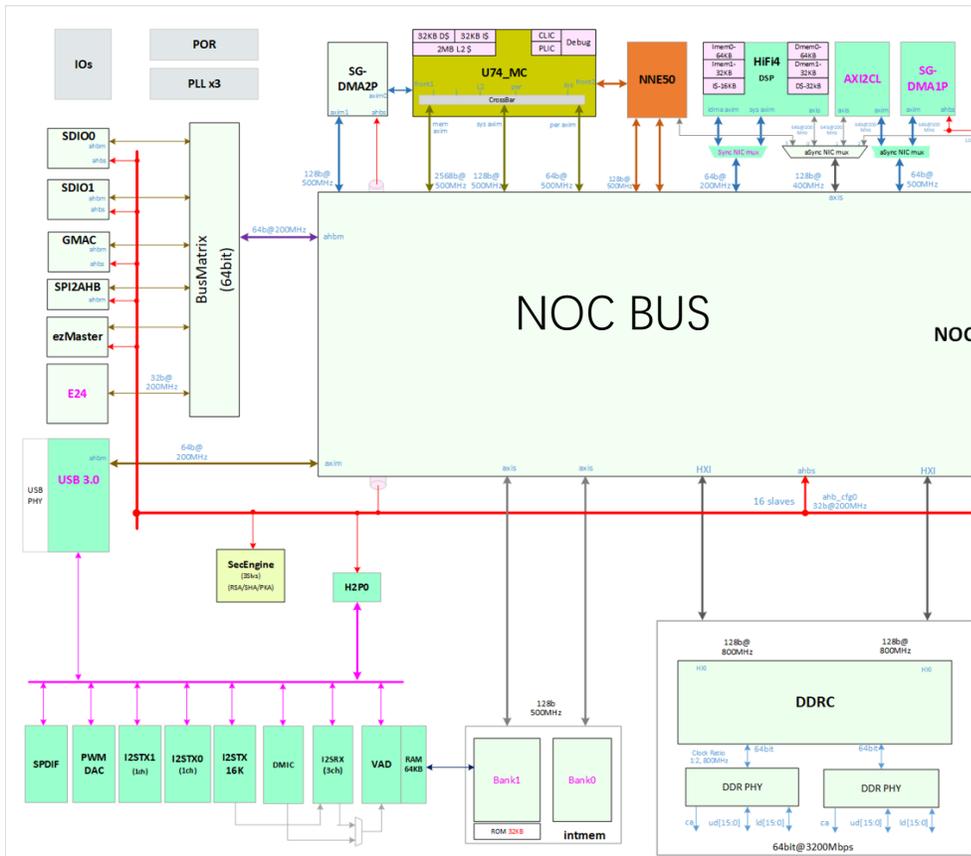


Port	Cacheable	Bursts	Atomics	Typical Use
Memory	✓	✓	✓	On-chip and/or off-chip cacheable, coherent memory. SCD supports up to 4 memory ports.
System		✓		High bandwidth, un-cached memory or devices
Peripheral			✓	Peripheral devices and low bandwidth memories
Front		✓		External Masters for accessing on Core Complex devices and ports. Transactions through the Front Port are coherent with L1/L2 Data Caches



Root causes - L2 Cache Coherence (JH7100 SOC)

- JH7100 main peripheral SDIO*,GMAC,USB3.0 connect NOC BUS directly, if any share data with CPU (U74), need flush L2 cache to keep cache coherency.
- There is a general DMA named SGDMA2P be connected to U74 CPU's front-port which will keep cache coherency automatically, peripheral data can use this DMA as a data share channel with CPU.





Software Workaround Solutions

- Now there are two registers in L2 cache controller which name Flush64 and Flush32 below. After Flush operation the cache line will be invalidated.

0x200	Flush64	Flush the physical address equal to the 64-bit written data from the cache
0x240	Flush32	Flush the physical address equal to the 32-bit written data << 4 from the cache

```
void stmmac_flush_dcache(unsigned long start, unsigned long len)
{
    unsigned long addr = _ALIGN_DOWN(start, 64);
    unsigned long lenth = len+start%64;

    starfive_flush_dcache(addr,lenth);
}
...

void starfive_flush_dcache(unsigned long start, unsigned long len)
{
    unsigned long line = start;
    unsigned long end = start+len;
    unsigned char *addr = (unsigned char *)dcache_addr+0x200;

    if(start < 0x80000000 || start > 0x87FFFFFF || end < 0x80000000 || end > 0x87FFFFFF)
        return;
    while(line < end){
        writeq(line, addr);
        line += 64;
        asm volatile ("fence");
    }
}
```

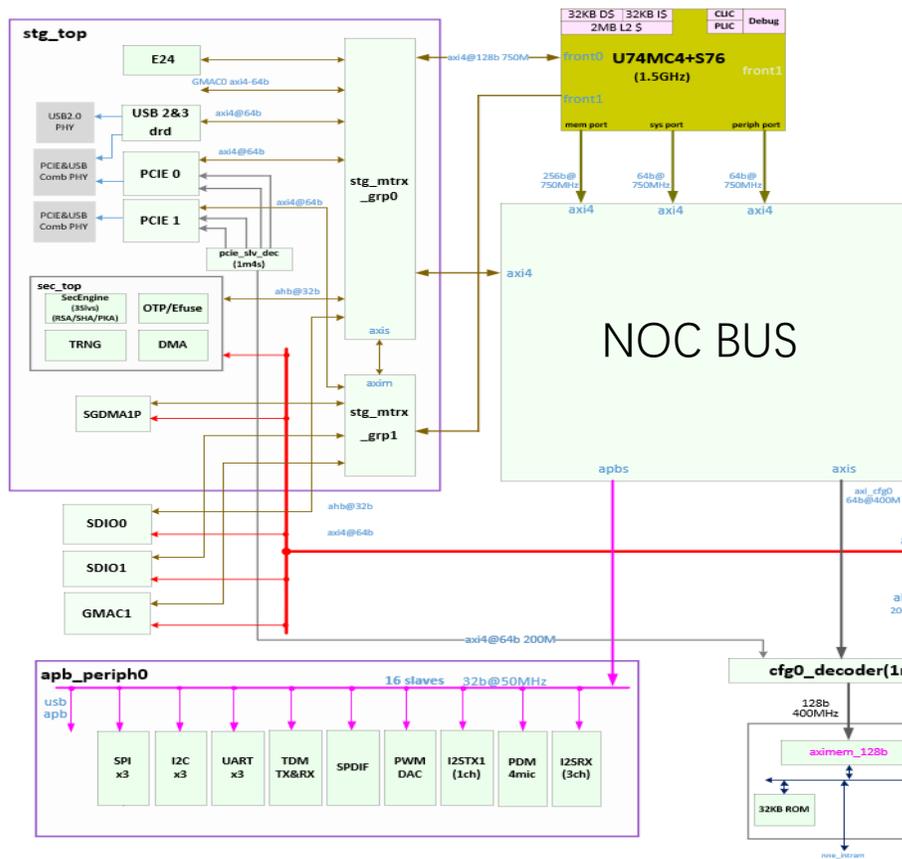
- “start” is the start of physical address, “len” is the length of memory which you want to flush.
- 1. Flush the cache line to DDR.
- 2. Invalidate the cache line.



Hardware Solution for JH7110 SOC

Next Generation SoC: JH7110 will solve the issue permanently via hardware

- JH7110 connect high speed peripheral to CPU front-port directly, which will keep cache coherency automatically.
- Low speed peripheral and video frame buffer data which need share data with CPU cacheable region could use DMA as data share channel with CPU cache.



JH7110

Index	IP Name	Description	Coherency	Solution
1	U74MC4+S76	CPU	Y	internal
2	VP6	Vision DSP	N	sys port
3	NNE50	AI engine	N	DMA/sys port
4	ISP+VIN	dual isp+vin	N	sys port
5	GPU	Imagination	N	sys port
6	VOUT	OSD/Overlay	N	sys port
7	WAVE511	H264/H265 Decoder/ IP support	N	sys port
8	WAVE521	H264/H265 Encoder/ IP support	N	sys port
9	JPEG	JPEG Codec	N	sys port
10	PCIe2.0 x2		Y	front port
11	USB3.0 x2	Host/Device	Y	front port
12	USB2.0 x1	OTG	Y	front port
13	GMACx2	Ethernet MAC -10M/100M/1000M	Y	front port
14	SDIOx2	SDIO X2	Y	front port
15	DMAc	DMA Controller	Y	front port
16	E24	co-processor	Y	front port
17	Security	SHA/ECC/AES	Y	front port
18	OTP		N	DMA
19	TRNG		N	DMA
20	UARTx6	UART x6	N	DMA
21	SPIx7	SPI x7	N	DMA
22	PWM	PWM x8	N	DMA
23	I2Cx7	I2C x7	N	DMA
24	VAD	Voice Activity Detector	N	DMA
25	TDM RX&TX		N	DMA
26	PWMDAC	PWMDAC x1	N	DMA
27	I2S	I2S x8	N	DMA
28	PDM	PDM x4	N	DMA
29	SPDIF	SPDIF x1	N	DMA
30	QSPI	nor or nand flash	N	
31	GPIO	GPIO x64	N	