

**U1000Y**  
RK3399

NC_1	AB22
NC_2	AD11
NC_3	AD12
NC_4	AC14
NC_5	AD14
NC_6	AD18
NC_7	AC12
NC_8	AA19
NC_9	AA20
NC_10	AB20
NC_11	AA22

Title: DevTerm A06 Core for Mainboard V3.14 Schematic

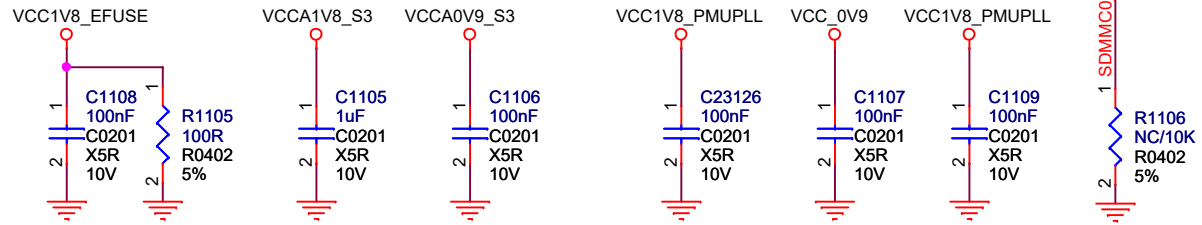
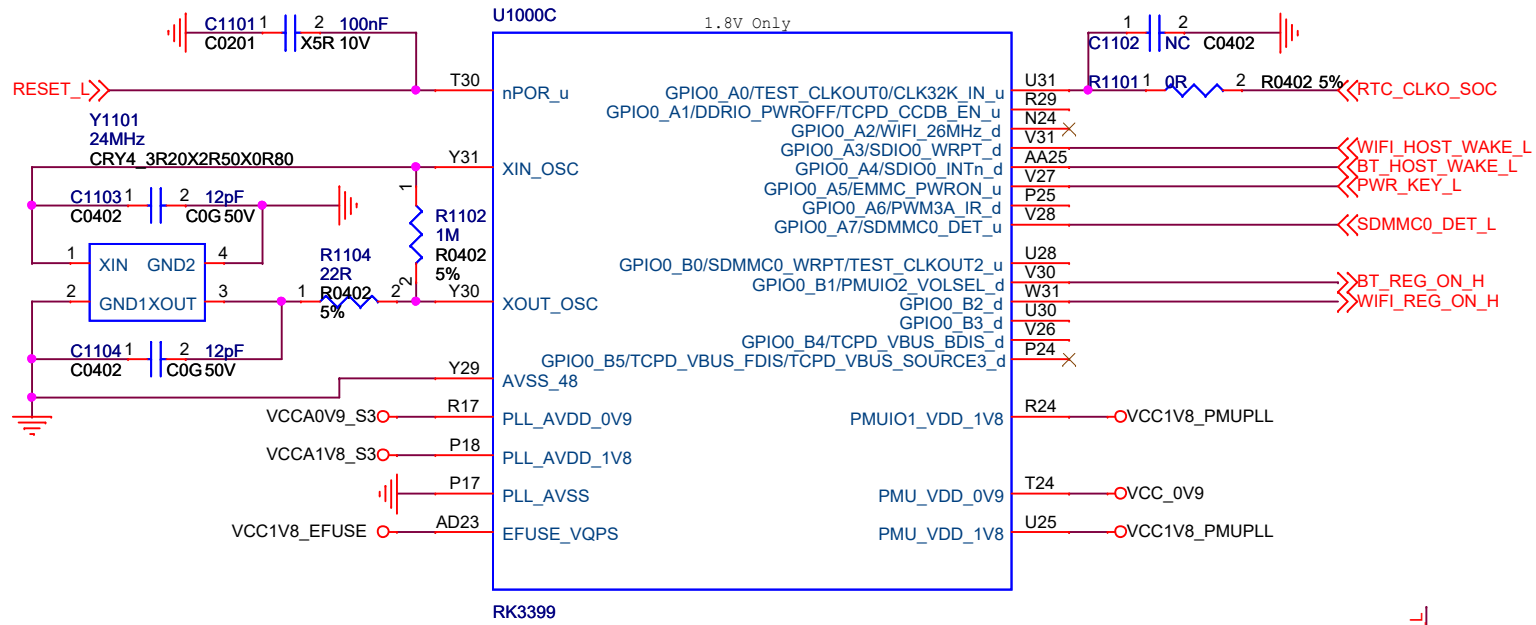
Size: A3

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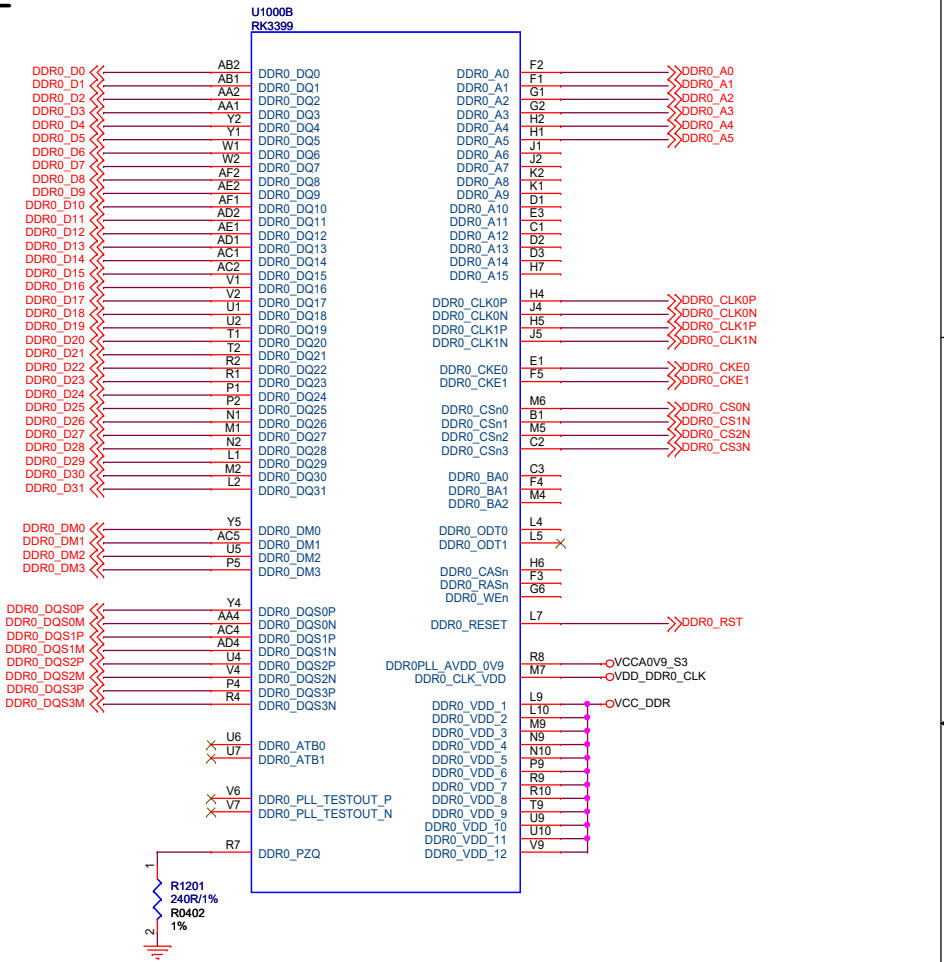
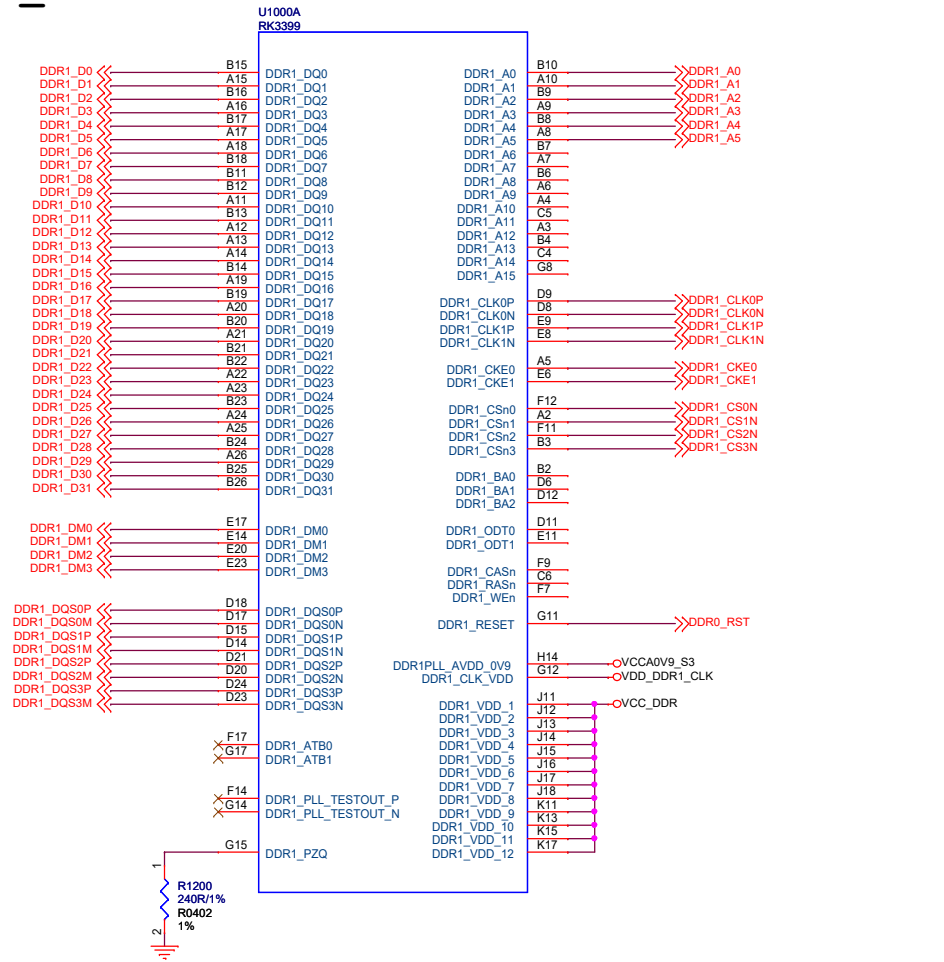
# RK3399\_C



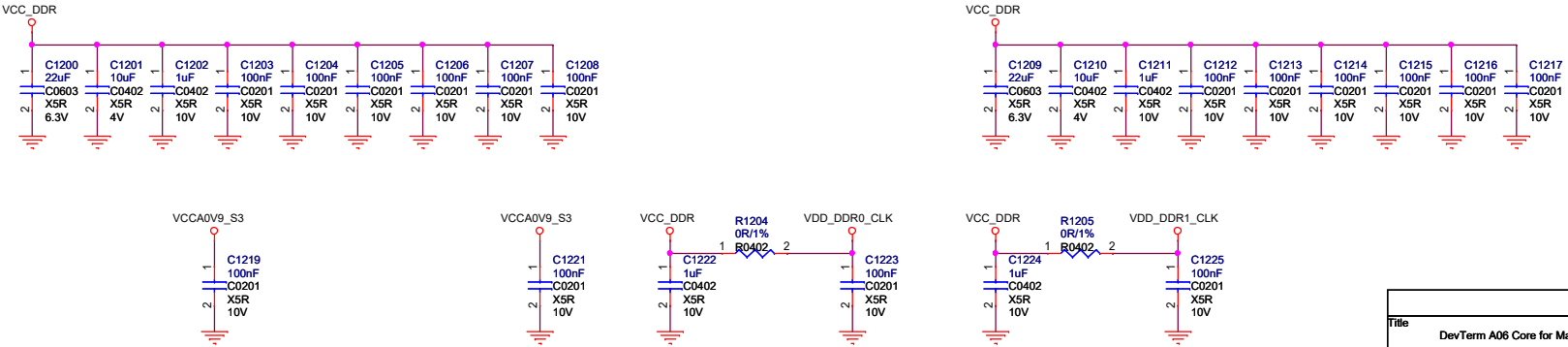
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# RK3399\_A

# RK3399\_B



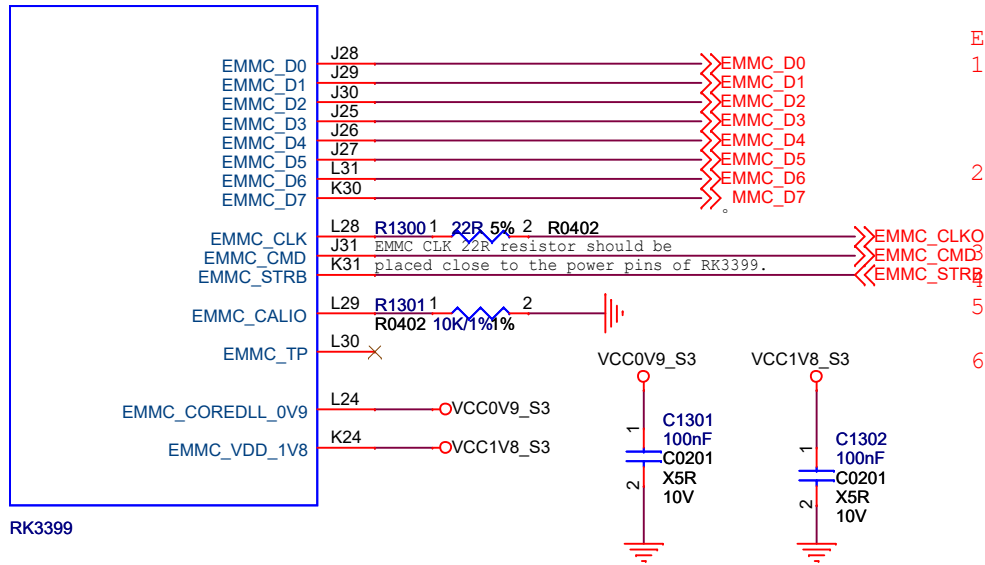
## DDR FILTER



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# RK3399\_H

U1000H



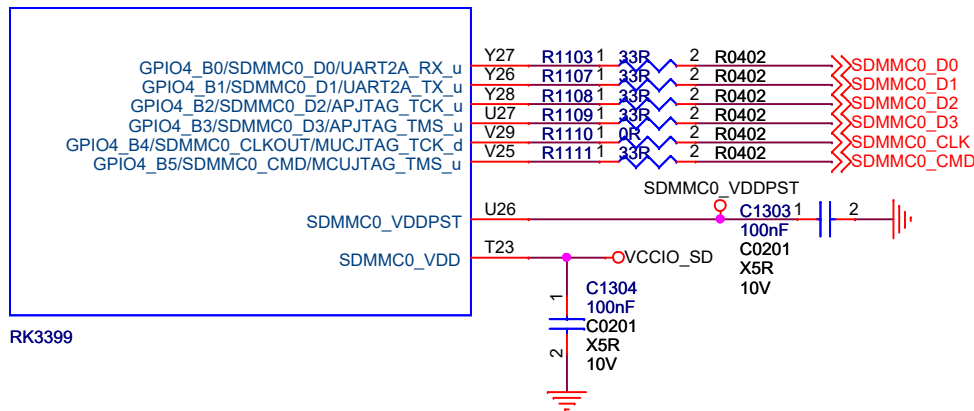
## EMMC design rules:

- 1.Data[0:3],CMD and Strobe lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
- 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
- 3.Max trace length < 3.93inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;
- 6.R1300 should be place close to RK3399;

Note:All the Power filter capacitors should be placed close to the power pins of RK3399

# RK3399\_F

U1000F



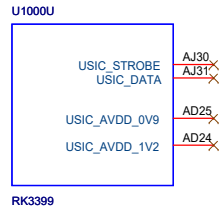
## SDMMC design rules:

- 1.Data[0:3] and CMD lines routing parallel as a group,and be isolated with other signals by GND line,the skew between group is less than 200mils;
- 2.Clk should be isolated with other signals by GND line;The skew between data signals is less than 20ps;
- 3.Max trace length < 3.93inches;
- 4.Trace impedance 50ohm+/-10%;
- 5.The distance between other signals follows the 3W rule;

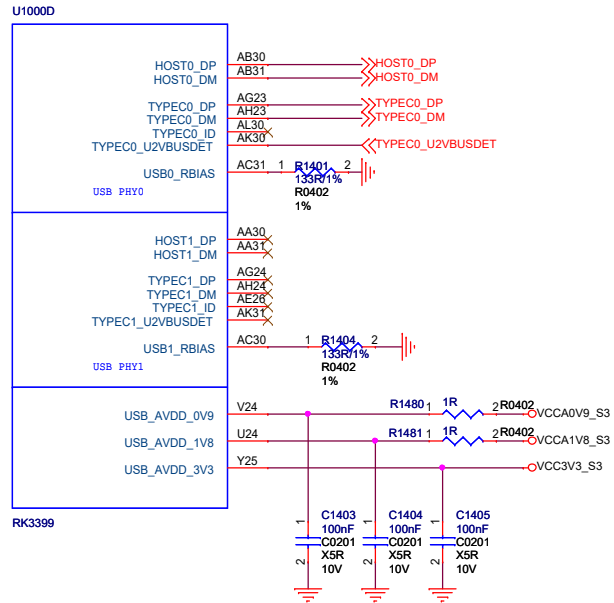
Note:All the Power filter capacitors should be placed close to the power pins of RK3399

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# RK3399\_U



# RK3399\_D

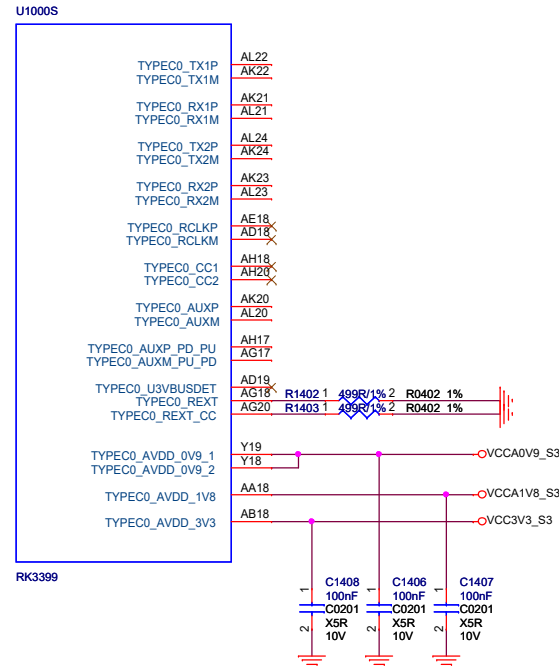


Note: All the Power filter capacitors should be placed close to the power pins of RK3399

### USB2.0 design rules:

1. Max intra-pair skew < 4ps;
2. Max trace length < 6inchs;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

# RK3399\_S

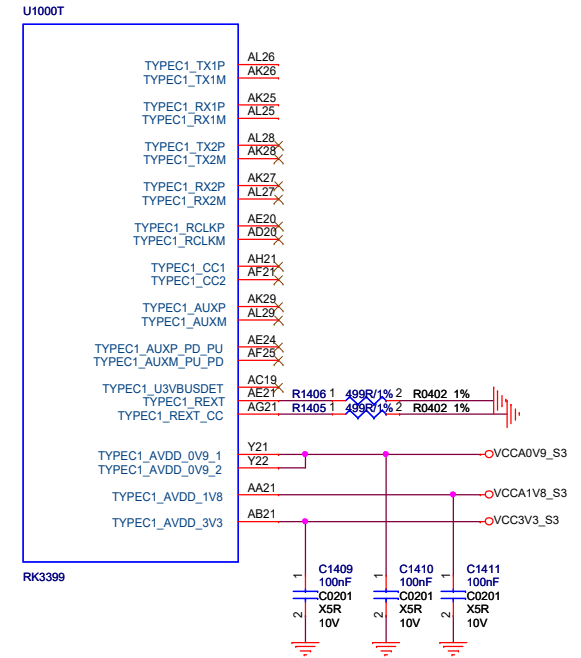


Note: All the Power filter capacitors should be placed close to the power pins of RK3399

### USB3.0 design rules:

1. Max intra-pair skew < 4ps;
2. Max length skew between TX and RX < 1.6ns;
3. Max trace length < 6inchs;
4. Max allowed via < 4;
5. Trace impedance 90ohm+/-10%;
6. The distance between other signals follows the 3W rule;

# RK3399\_T

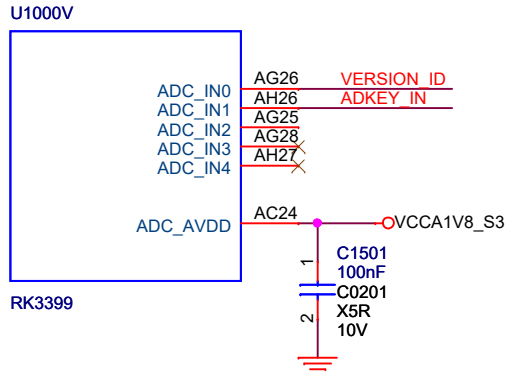


### DP design rules:

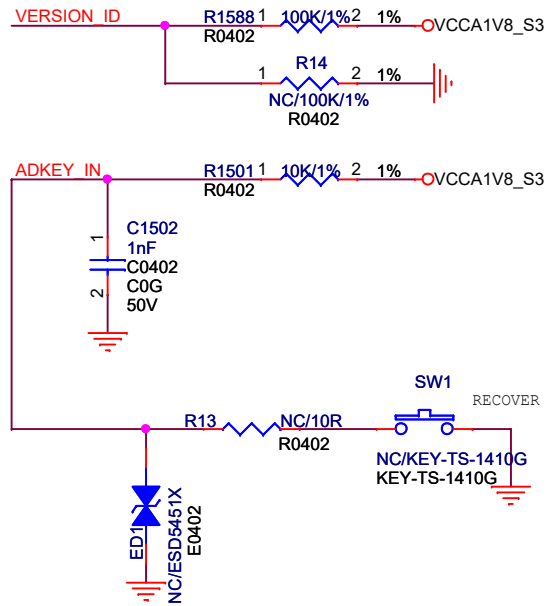
1. Max intra-pair skew < 4ps;
2. Max trace length < 6inchs;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

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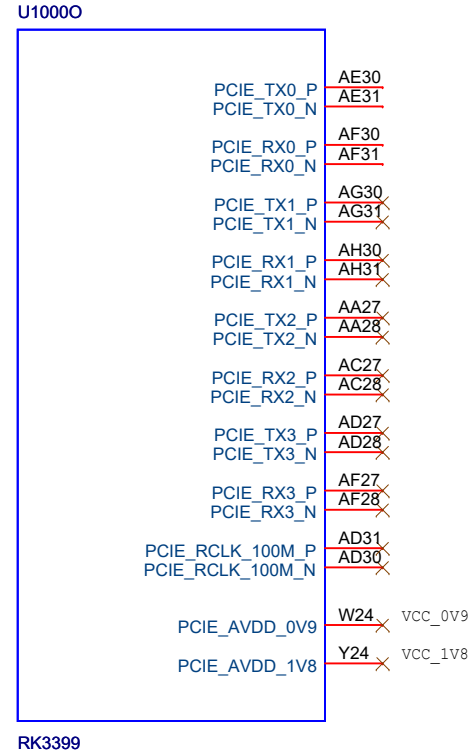
# RK3399\_V



Note: All the Power filter capacitors should be placed close to the power pins of RK3399



# RK3399\_O



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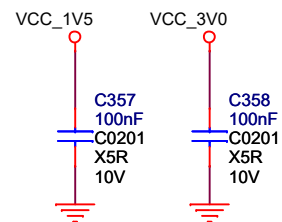
# RK3399\_L

U1000L

GPIO2\_A0/VOP\_D0/CIF\_D0/I2C2\_SDA\_u  
 GPIO2\_A1/VOP\_D1/CIF\_D1/I2C2\_SCL\_u  
 GPIO2\_A2/VOP\_D2/CIF\_D2\_d  
 GPIO2\_A3/VOP\_D3/CIF\_D3\_d  
 GPIO2\_A4/VOP\_D4/CIF\_D4\_d  
 GPIO2\_A5/VOP\_D5/CIF\_D5\_d  
 GPIO2\_A6/VOP\_D6/CIF\_D6\_d  
 GPIO2\_A7/VOP\_D7/CIF\_D7/I2C7\_SDA\_u  
  
 GPIO2\_B0/VOP\_CLK/CIF\_VSYNC/I2C7\_SCL\_u  
 GPIO2\_B1/SPI2\_RXD/CIF\_HREF/I2C6\_SDA\_u  
 GPIO2\_B2/SPI2\_TXD/CIF\_CLKIN/I2C6\_SCL\_u  
 GPIO2\_B3/SPI2\_CLK/VOP\_DEN/CIF\_CLKOUTA\_u  
 GPIO2\_B4/SPI2\_CS\_n0\_u

G31 >> I2C2\_SDA/GPIO2\_A0\_U  
 H25 >> I2C2\_SCL/GPIO2\_A1\_U  
 H30  
 F28  
 H29  
 F29  
 H27  
 G30

H28  
 F30  
 H24  
 H31  
 F31  
  
 J24 -> VCC\_1V5  
 K23 -> VCC\_3V0



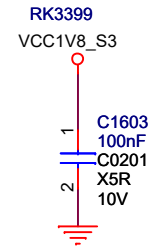
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The power domain can be designed to be 1.8V or 3.0v.  
 It should be noted that software configuration needs to be consistent with hardware design.

# RK3399\_R

U1000R

MIPI\_RX0\_D0P AK15 >> MIPI\_RX0\_D0P  
 MIPI\_RX0\_D0N AL15 >> MIPI\_RX0\_D0N  
  
 MIPI\_RX0\_D1P AK14 >> MIPI\_RX0\_D1P  
 MIPI\_RX0\_D1N AL14 >> MIPI\_RX0\_D1N  
  
 MIPI\_RX0\_CLKP AK13 >> MIPI\_RX0\_CLKP  
 MIPI\_RX0\_CLKN AL13 >> MIPI\_RX0\_CLKN  
  
 MIPI\_RX0\_D2P AK12 >> MIPI\_RX0\_D2P  
 MIPI\_RX0\_D2N AL12 >> MIPI\_RX0\_D2N  
  
 MIPI\_RX0\_D3P AK11 >> MIPI\_RX0\_D3P  
 MIPI\_RX0\_D3N AL11 >> MIPI\_RX0\_D3N  
  
 MIPI\_RX0\_REXT AF14 R1605 1 4.02K 1% R0402 1%  
  
 MIPI\_RX0\_AVDD\_1V8 AB14 -> VCC1V8\_S3



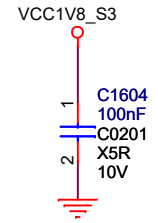
RK3399

# RK3399\_P

U1000P

MIPI\_TX1/RX1\_D0P AK6 >> MIPI\_TX1/RX1\_D0P  
 MIPI\_TX1/RX1\_D0N AL6 >> MIPI\_TX1/RX1\_D0N  
  
 MIPI\_TX1/RX1\_D1P AK7 >> MIPI\_TX1/RX1\_D1P  
 MIPI\_TX1/RX1\_D1N AL7 >> MIPI\_TX1/RX1\_D1N  
  
 MIPI\_TX1/RX1\_CLKP AK8 >> MIPI\_TX1/RX1\_CLKP  
 MIPI\_TX1/RX1\_CLKN AL8 >> MIPI\_TX1/RX1\_CLKN  
  
 MIPI\_TX1/RX1\_D2P AK9  
 MIPI\_TX1/RX1\_D2N AL9  
  
 MIPI\_TX1/RX1\_D3P AK10  
 MIPI\_TX1/RX1\_D3N AL10  
  
 MIPI\_TX1/RX1\_REXT AF11 R1606 1 4.02K 1% R0402 1%  
  
 MIPI\_TX1/RX1\_AVDD\_1V8 AC10 -> VCC1V8\_S3

- MIPI design rules:
1. Max intra-pair skew < 4ps;
  2. Max length skew between clk and data < 7ps;
  3. Max trace length < 7.2inches;
  4. Max allowed via < 4;
  5. Trace impedance 100ohm+/-10%;
  6. The distance between other signals follows the 3W rule;

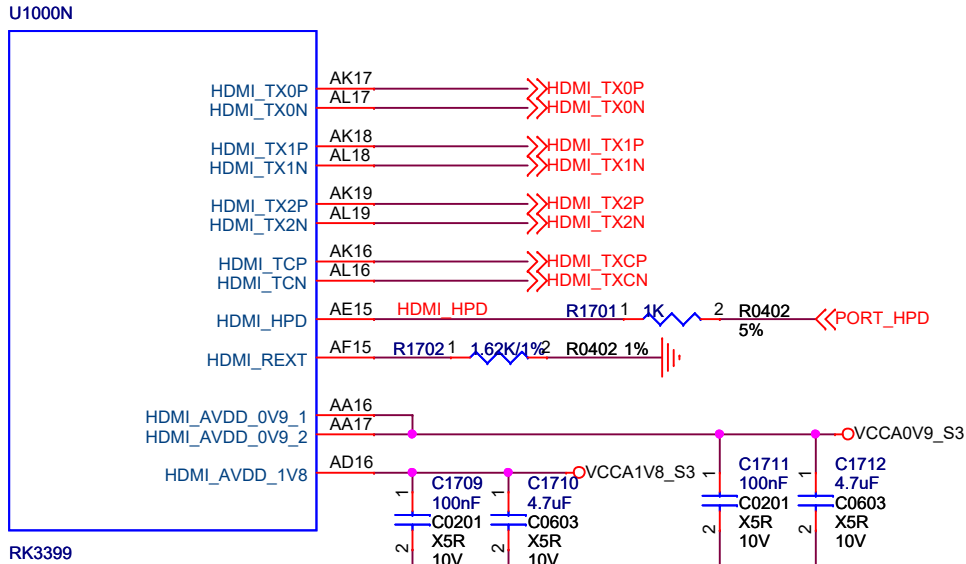


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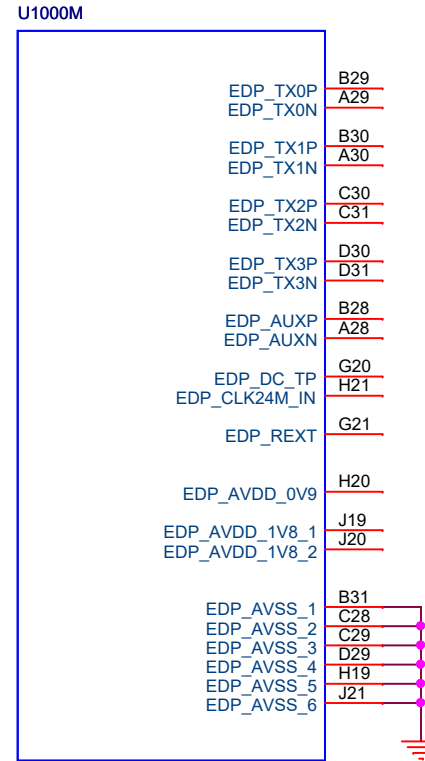
# RK3399\_N



## HDMI design rules:

1. Max intra-pair skew < 4ps;
2. Max length skew between clk and data < 80ps;
3. Max trace length < 9.8inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. The distance between other signals follows the 3W rule;

# RK3399\_M



RK3399

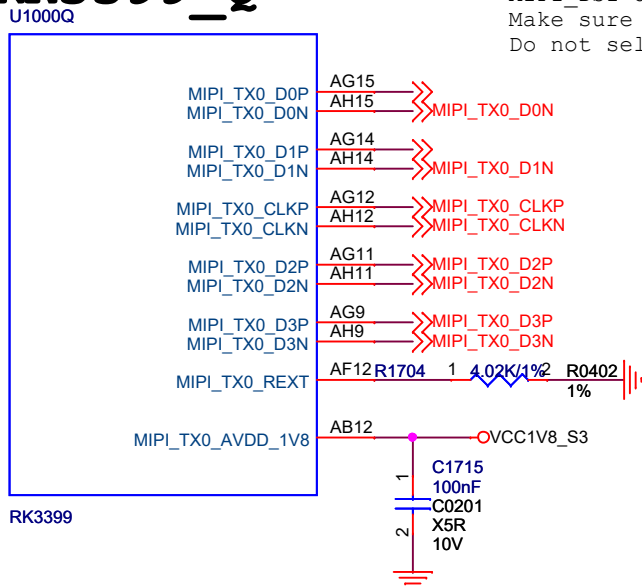
## eDP design rules:

1. Max intra-pair skew < 4 ps;
2. Max trace length < 6inches;
3. Max allowed via < 4;
4. Trace impedance 90ohm+/-10%;
5. The distance between other signals follows the 3W rule;

## MIPI design rule:

1. Max intra-pair skew < 4 ps;
2. Max length skew between clk and data < 7ps;
3. Max trace length < 7.2 inches;
4. Max allowed via < 4;
5. Trace impedance 100ohm+/-10%;
6. The distance between other signals follows the 3W rule;

# RK3399\_Q

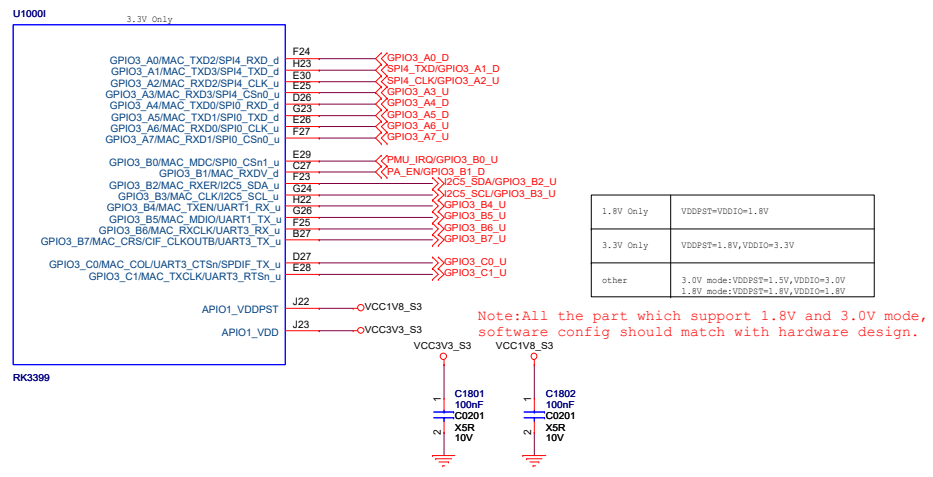


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The product definition is a single MIPI\_DSI display screen.  
Make sure you choose the MIPI\_TX0 channel.  
Do not select the MIPI\_TX1/RX1 channel.

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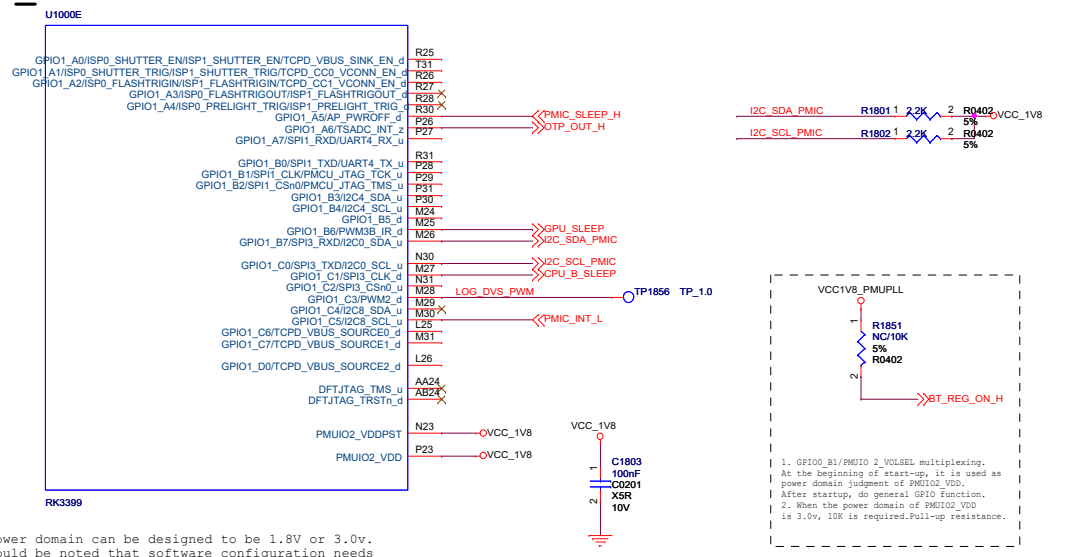
# RK3399\_I



Note: All the part which support 1.8V and 3.0V mode, software config should match with hardware design.

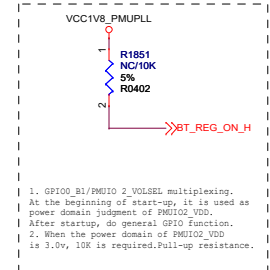
Note: All the Power filter capacitors should be placed close to the power pins of RK3399

# RK3399\_E



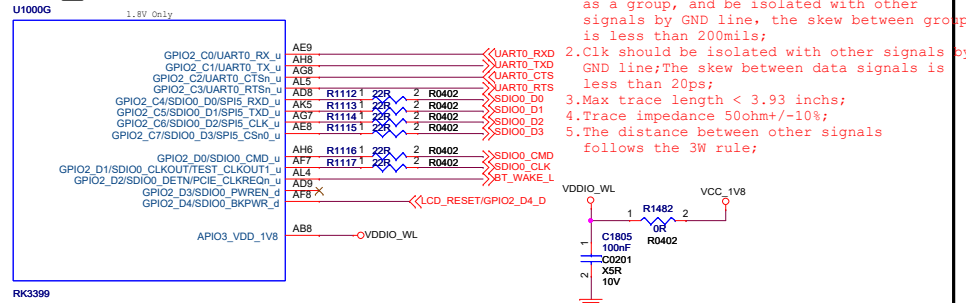
The power domain can be designed to be 1.8V or 3.0V. It should be noted that software configuration needs to be consistent with hardware design.

Note: All the Power filter capacitors should be placed close to the power pins of RK3399



1. GPIO0\_B1/PMIO2\_2\_VOLSEL multiplexing. At the beginning of start-up, it is used as power domain judgment of PMIO2\_VDD. After startup, do general GPIO Function.
2. When the power domain of PMIO2\_VDD is 3.0v, 10K is required. Pull-up resistance.

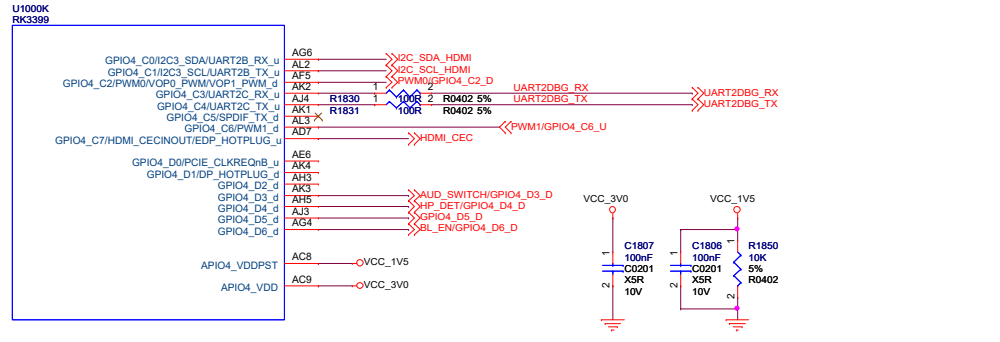
# RK3399\_G



- SDIO design rules:
1. Data[0:3] and CMD lines routing parallel as a group, and be isolated with other signals by GND line, the skew between group is less than 200mils;
  2. CLK should be isolated with other signals by GND line; The skew between data signals is less than 20ps;
  3. Max trace length < 3.93 inches;
  4. Trace impedance 50ohm +/- 10%;
  5. The distance between other signals follows the 3W rule;

Note: All the Power filter capacitors should be placed close to the power pins of RK3399

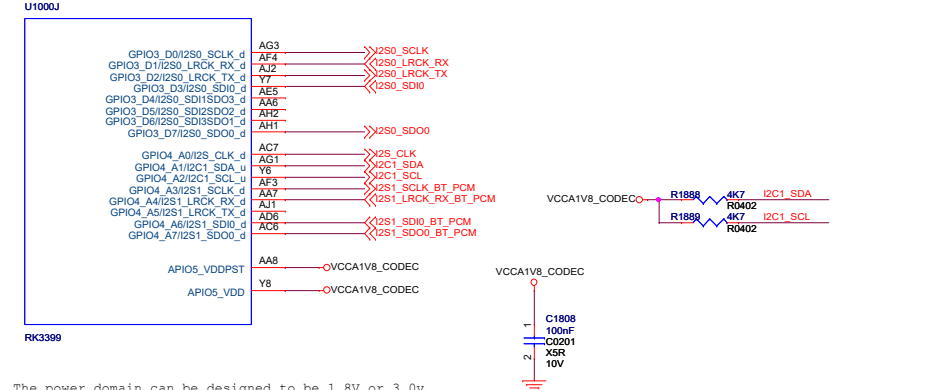
# RK3399\_K



The power domain can be designed to be 1.8V or 3.0V. It should be noted that software configuration needs to be consistent with hardware design.

Note: All the Power filter capacitors should be placed close to the power pins of RK3399

# RK3399\_J



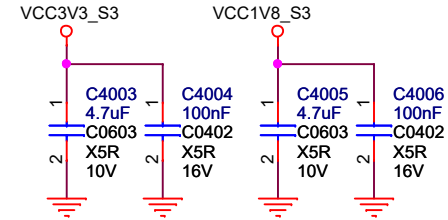
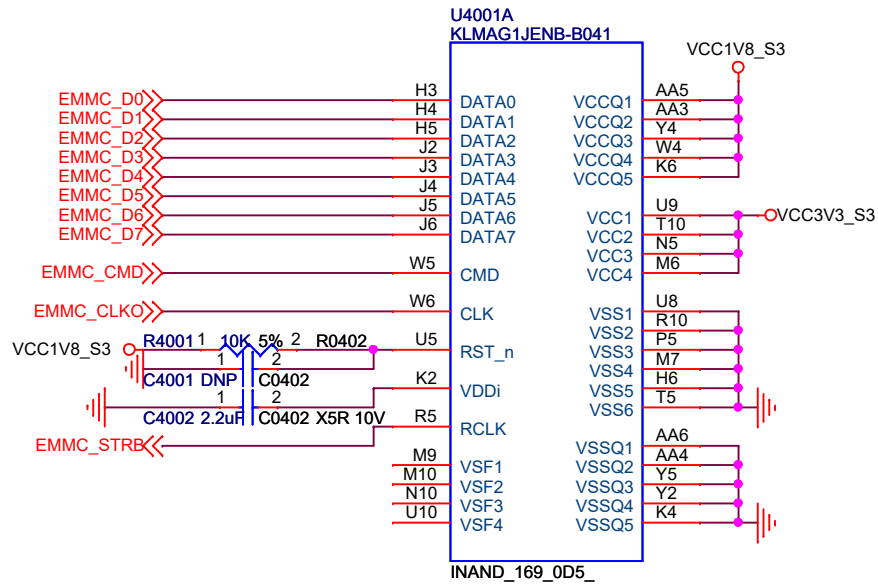
Note: All the Power filter capacitors should be placed close to the power pins of RK3399

The power domain can be designed to be 1.8V or 3.0V. It should be noted that software configuration needs to be consistent with hardware design.

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# eMMC FLASH

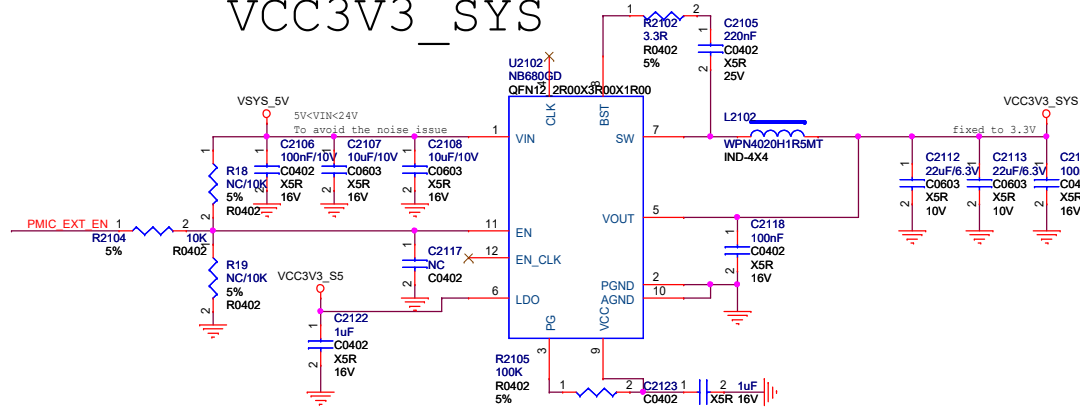


Note: All the Power filter capacitors should be placed close to the power pins of eMMC

Note:  
Reserve TestPoint for firmware update.  
If EMMC\_CLKO=0V at power-on reset,  
then system will enter into Maskrom mode.

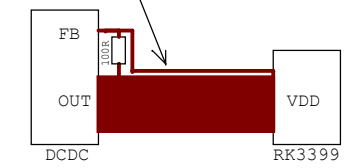
# VCC3V3\_SYS

CLOCKWORK

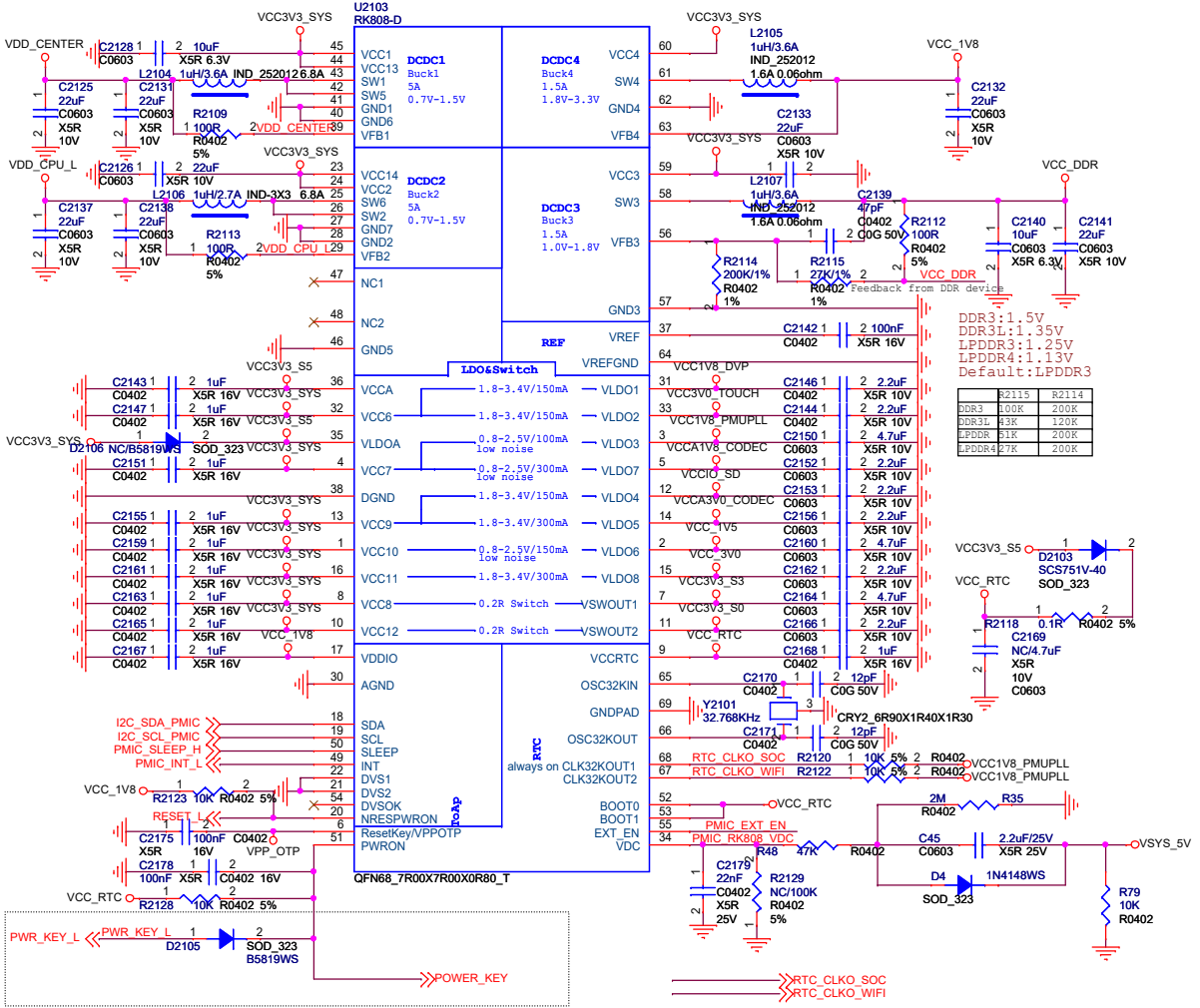


- 1, VDD\_CPU\_L
- 2, VDD\_CENTER
- 3, VCC\_DDR
- 4, VDD\_CPU\_B
- 5, VDD\_GPU
- 6, VDD\_LOG

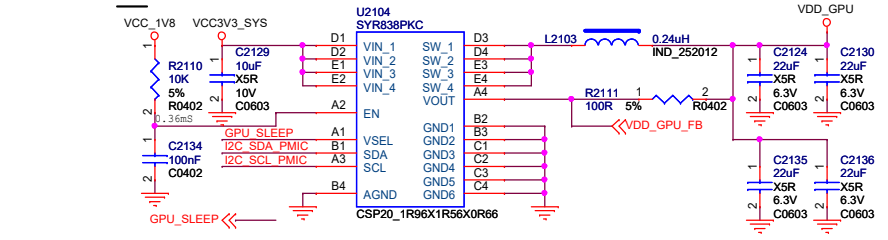
Feedback from RK3399



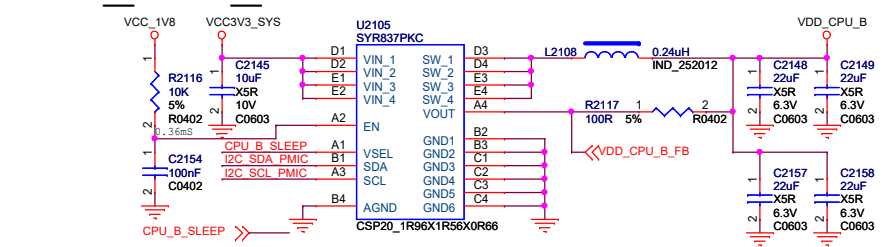
# PMIC RK808-D



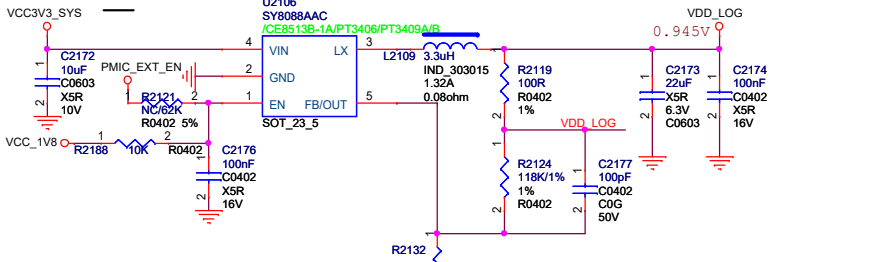
# VDD\_GPU



# VDD\_CPU\_B



# VDD\_LOG



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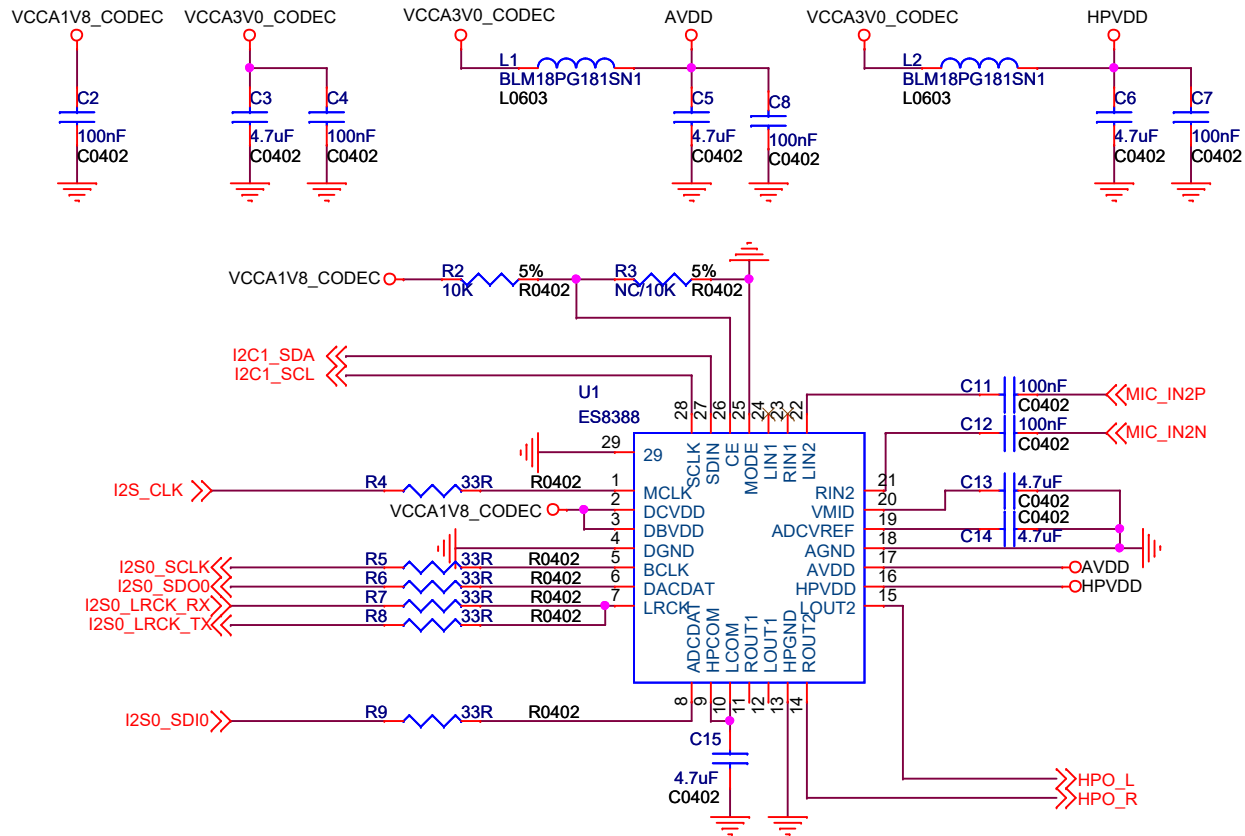
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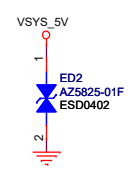
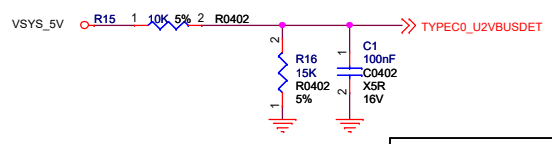
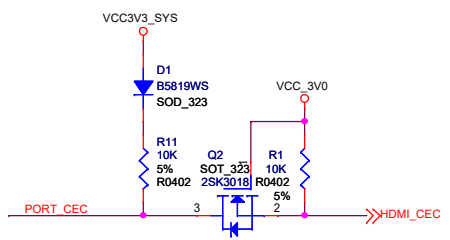
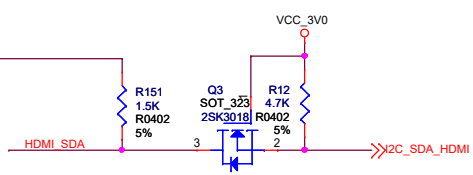
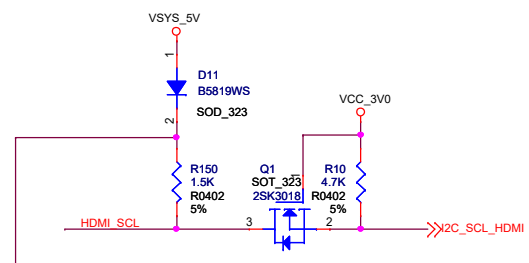
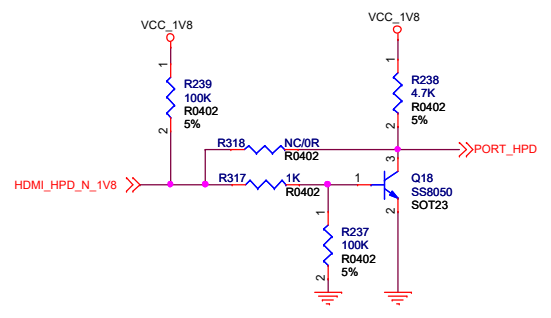
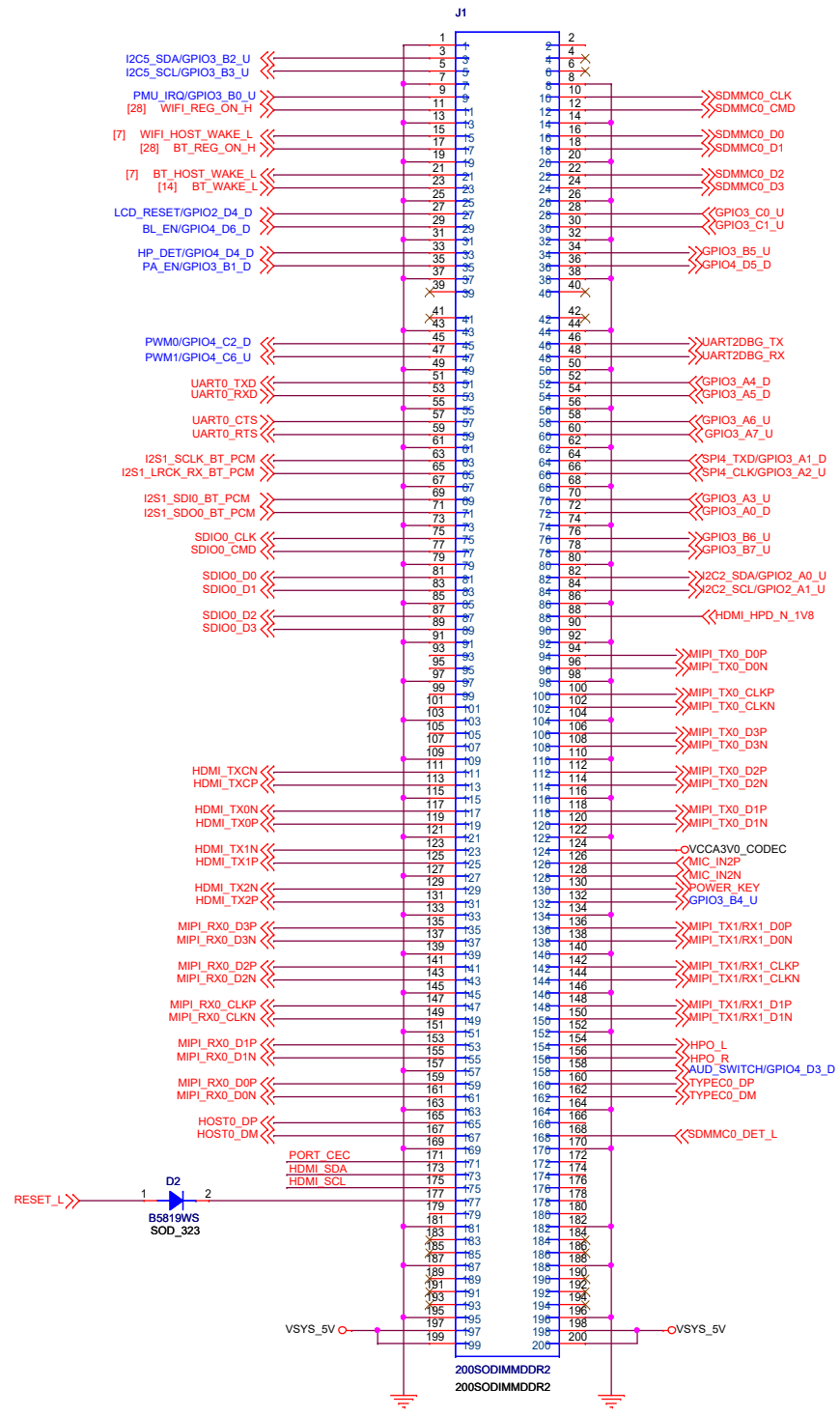
Rev: 2




# CODEC



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