α-Si TFT Mobile Display Driver IC Specification

ICNL9707

Specification Version

Model： ICNL9707

Document Version： V0.01

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Chipone Technology (Beijing) Co.,Ltd.

Index

1. Description

This document describes Chipone's ICNL9707 is an integrated chip of amorphous-silicon (a-si) thin film transistor (TFT) LCD display controllers, and supports 720/640/600 (RGB) resolution. It includes a timing controller with glass interface level-shifters and a glass power supply circuit to drive a dot-matrix TFT LCD.

ICNL9707 supports MIPI DSI (Display Serial Interface) interface mode, and support 550 Mbps per lane at 4 data lanes application on MIPI DSI.

ICNL9707 is suitable for general small portable battery-driven and long-term driving products, such as digital cellular phones, smart phones.

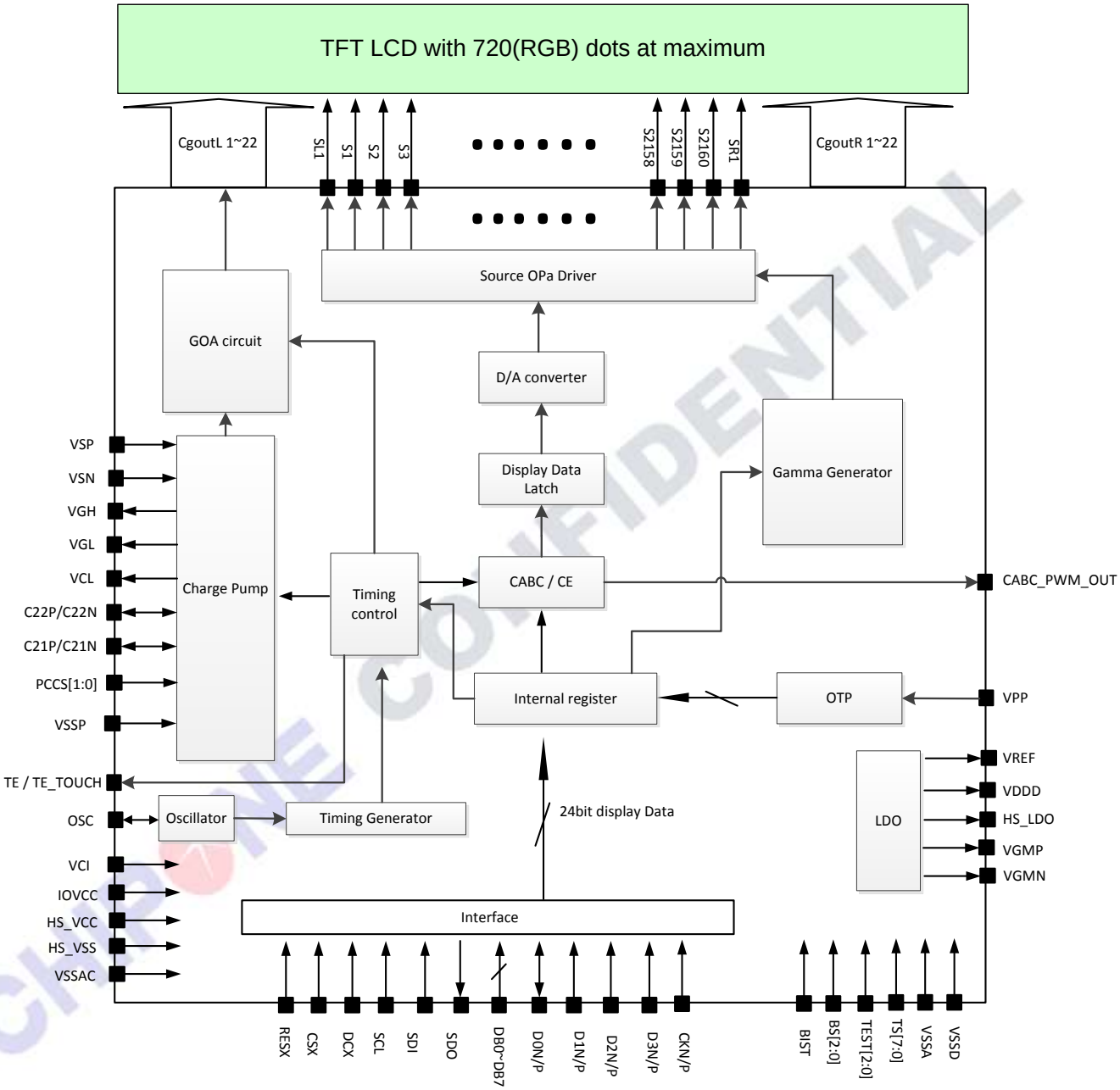
2. Features

1. Single chip RAM-less α-Si TFT LCD Driver and supports display resolution:
   - 720 RGB × (2 × NL)
   - 640 RGB × (2 × NL)
   - 600 RGB × (2 × NL)
2. Interface:
   - MIPI Display Serial Interface (DSI V1.01 r11 and D-PHY V1.0)
   - MIPI Data rate:
     i. Max 550Mbps/lane at 4 lane application.
     ii. Max 600Mbps/lane at 3 lane application.
3. Display color modes:
   - Support full color mode 16.7M colors.
4. Panel driving:
   - 2162 source outputs.
   - CGOUTL 1~22 and CGOUTR 1~22 pads for GIP timings control.
   - 1 dot / 2 dot / 4 dot / 8 dot / Column and Zig-Zag inversion type.
   - DC VCOM voltage generator and adjustment.
5. Output voltage level:
   - Positive gamma high voltage range for **VGMP.**
   - Negative gamma low voltage range for **VGMN.**
   - GIP timings control voltage range for **VGL** to **VGH.**
   - Common electrode voltage range for **VCOM.**
6. Input voltage level:
   - Logic and interface power supply (**IOVCC**).
   - Analog power supply (**VCI).**
   - Positive source driver power supply (**VSP**).
   - Negative source driver power supply (**VSN**).
   - OTP programming voltage (**VPP**).
7. On-chip functions:
   - Internal oscillator for display clock generation.
   - Support **CABC** (Content Adaptive Brightness Control) function.
   - Support **CE** (Color Enhancement) function.
   - Support **Notch** function

- Support **DGC** (Digital Gamma Control) function.
- **VGH/VGL** voltage generator for TFT panel gate control.
- Support 1 time OTP (One-Time Programming) for initial setting registers.
- Support 3 times OTP for **VCOM.**
- Support 3 times OTP for **ID 1/2/3**.
- Support 2 times OTP for **DGC setting**.

3. Device Overview

3.1 Block diagram



3.2 Pin description

3.2.1 Power Input Pads

Symbol	Pad Type	Description
VCI	Power Supply	Power supply to the analog circuit.
IOVCC	Power Supply	Power supply for the logic power and I/O circuit.
HS_VCC	Power Supply	Power supply for MIPI D-PHY analog power.
VSP	Power Supply	Power supply for Charge pump circuit.
VSN	Power Supply	Power supply for Charge pump circuit.
VPP	Power Supply	Power supply for OTP.
VSSP	Power Supply	Charge Pump circuit ground.
VSSD	Power Supply	Logic power and I/O circuit ground.
VSSAC	Power Supply	Analog circuit ground.
HS_VSS	Power Supply	MIPI High speed circuit ground.
VSSA	Power Supply	Analog circuit ground.

3.2.2 Power Output Pads

Symbol	Pad Type	Description
HS_LDO	Analog output	LDO output for MIPI.
VDDD	Analog output	LDO output for Digital circuit. It must be connected a stabilizing capacitor 1.0uF to VSS.
VCL	Analog pump	Voltage for Level shift and VCOM
VGH	Analog pump	Voltage for Panel TFT. It must be connected a stabilizing capacitor 1.0uF to VSS.
VGL	Analog pump	Voltage for Panel TFT. It must be connected a stabilizing capacitor 1.0uF to VSS.
VGMP	Analog output	LDO output for Positive Gamma.
VGMN	Analog output	LDO output for Negative Gamma.
VCOM	Analog output	LDO output for Panel common. It must be connected a stabilizing capacitor 1.0uF to VSS.
VREF	Analog output	Analog refer power.
C21P / N	Charge pump	Connect to the step-up capacitors for VGH voltage.
C22P / N	Charge pump	Connect to the step-up capacitors for VGH voltage.
VCSW1 / 2	Analog output	Analog clock phase output for PMIC
CgoutL 1~22	Analog output	GOA circuit output for Panel TFT.
CgoutR 1~22	Analog output	GOA circuit output for Panel TFT.
S1~S2160	Analog output	Analog output for Panel TFT source
SL1, SR1	Analog output	Analog output for Panel TFT ZigZag source

3.2.3 Digital Interface Output Pads

Symbol	Pad Type	Description
CABC_PWM_OUT	Digital output	Backlight control pin. This pin connect to external LED driver IC.
TE	Digital output	Tearing Effect pin.
TE_TOUCH	Digital output	Tearing Effect pin. (Each scan line).

3.2.4 Digital Interface Input Pads

<table>
<tr><th>Symbol</th><th>Pad Type</th><th>Description</th></tr>
<tr><td>RESX</td><td>Input</td><td>This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.</td></tr>
<tr><td>PCCS1/
PCCS0</td><td>Digital Input</td><td>Select the power mode method as listed below.
<table>
<tr><th>PCCS [1:0]</th><th>IOVCC</th><th>VCI</th><th>VSP</th><th>VSN</th><th>VGH/VGL</th></tr>
<tr><td>10</td><td>External</td><td>External</td><td>PMIC</td><td>PMIC</td><td>Internal</td></tr>
<tr><td>11</td><td>External</td><td>X</td><td>External</td><td>External</td><td>Internal</td></tr>
</table></td></tr>
<tr><td>BS2/
BS1/
BS0</td><td>Digital Input</td><td>BS[2:0] are used for the combination of polarity swap and data lane swap of DSI. Input mode method as listed below.
<table>
<tr><th>BS [2:0]</th><th>HS_CKN</th><th>HS_CKP</th><th>HS_D0N</th><th>HS_D0P</th><th>HS_D1N</th><th>HS_D1P</th><th>HS_D2N</th><th>HS_D2P</th><th>HS_D3N</th><th>HS_D3P</th></tr>
<tr><td>000</td><td>CKN</td><td>CKP</td><td>D3N</td><td>D3P</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td></tr>
<tr><td>001</td><td>CKP</td><td>CKN</td><td>D3P</td><td>D3N</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td></tr>
<tr><td>010</td><td>CKN</td><td>CKP</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>011</td><td>CKP</td><td>CKN</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>100</td><td>CKN</td><td>CKP</td><td>D2N</td><td>D2P</td><td>D1N</td><td>D1P</td><td>D0N</td><td>D0P</td><td>D3N</td><td>D3P</td></tr>
<tr><td>101</td><td>CKP</td><td>CKN</td><td>D2P</td><td>D2N</td><td>D1P</td><td>D1N</td><td>D0P</td><td>D0N</td><td>D3P</td><td>D3N</td></tr>
<tr><td>110</td><td>CKN</td><td>CKP</td><td>D3N</td><td>D3P</td><td>D0N</td><td>D0P</td><td>D1N</td><td>D1P</td><td>D2N</td><td>D2P</td></tr>
<tr><td>111</td><td>CKP</td><td>CKN</td><td>D3P</td><td>D3N</td><td>D0P</td><td>D0N</td><td>D1P</td><td>D1N</td><td>D2P</td><td>D2N</td></tr>
</table></td></tr>
</table>

3.2.5 MIPI Interface Pads

Symbol	Pad Type	Description
HS_D0N/P	Digital I/O	MIPI-DSI Data differential signal input / Output pins.
HS_D1N/P	Digital Input	MIPI-DSI Data differential signal input pins.
HS_D2N/P	Digital Input	MIPI-DSI Data differential signal input pins.
HS_D3N/P	Digital Input	MIPI-DSI Data differential signal input pins.
HS_CKN/P	Digital Input	MIPI-DSI Clock differential signal input pins.

3.2.6 Test Pads

Symbol	Pad Type	Description
VTESTOUTN	Analog test pad	Test mode for Gamma voltage output. This pin can be open.
VTSETOUTP	Analog test pad	Test mode for Gamma voltage output. This pin can be open.
TS[7:0]	Digital test pad	Test mode for Internal Logic function test. This pin can be open.
TEST_OSC	Digital test pad	Test mode for Oscillator input for test purpose. This pin can be open or connect to VSSD.
DB[7:0]	Digital test pad	Test mode for Data Bus signals. This pin can be open
BIST	Digital test pad	Internal Logic function test. This pin can be open
DCX	Digital test pad	Test mode for Select Command / Data This pin connects to IOVCC or VSSD..
CSX	Digital test pad	Test mode for Chip select. This pin connects to IOVCC.
SCL	Digital test pad	Test mode for Serial clock input. This pin connects to IOVCC.
SDI	Digital test pad	Test mode for Serial data input. This pin can be open.
SDO	Digital test pad	Test mode for Serial data output. This pin can be open.
TEST[2:0]	Digital test pad	Test mode for Internal Logic function test. This pin can be open or connect to VSSD.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

The absolute maximum rating is listed in below table. It may lead permanently damaged when ICNL9707 is used out of the absolute maximum rating.

To use ICNL9707 within the following electrical characteristics is strongly recommended for normal operation. ICNL9707 will malfunction and be poor reliability when these electrical characteristic conditions are exceeded during normal operation.

Table 4-1 Absolute maximum rating

Item	Symbol	Rating			Unit
		Min.	Typ.	Max.	
Supply voltage	IOVCC ~ VSSD	-0.3	-	(TBD)	V
Supply voltage	VCI ~ VSSA	-0.3	-	+6.6	V
Supply voltage	HS_VCC ~ HS_VSS	-0.3	-	(TBD)	V
Supply voltage	VSP ~ VSSA	-0.3	-	+6.6	V
Supply voltage	VSSA ~ VSN	-6.6	-	0	V
Supply voltage	VGH ~ VGL	|VGH-VGL| ≦30			V
Operating temperature	Topr	-40		+85	℃
Storage temperature	Tstg	-55		+110	℃
Input voltage	Vin	-0.3		IOVCC+0.3	V
HS input voltage	Vhsin	-0.3		+2	V

4.2 DC Characteristics

Condition : Ta =25℃

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Power generation & Operation Voltage							
Analog Operating voltage	VCI	Operating Voltage	(TBD)	-	(TBD)	V	1
Analog Operating voltage	VSP	Operating Voltage	(TBD)	-	(TBD)	V	
Analog Operating voltage	VSN	Operating Voltage	(TBD)	-	(TBD)	V	
Analog Operating voltage	VCOM	Operating Voltage	(TBD)	-	(TBD)	V	
Analog Operating voltage	VGMP	Operating Voltage	(TBD)	-	(TBD)	V	
Analog Operating voltage	VGMN	Operating Voltage	(TBD)	-	(TBD)	V	
Analog Operating voltage	|VGH-VGL|	Operating Voltage	|VGH-VGL| ≦30			V	
I/O operating voltage	IOVCC	I/O supply voltage	(TBD)	(TBD)	(TBD)	V	
MIPI Operating voltage	HS_VCC	HSVCC supply voltage	(TBD)	(TBD)	(TBD)	V	
LOGIC INPUT/ OUTPUT							
Logic High level input voltage	VIH		0.7× IOVCC	-	IOVCC	V	2
Logic Low level input voltage	VIL	-	VSS	-	0.3× IOVCC	V	2
Logic High level output voltage	VOH	IOH = -0.1mA	0.8× IOVCC	-	IOVCC	V	3
Logic Low level output voltage	VOL	IOL = +0.1mA	VSS	-	0.2× IOVCC	V	3
Logic High level leakage	ILIH1	Vin = 0 to IOVCC	-	-	1	μA	2,3
Logic Low level leakage	ILIL1	Vin = 0 to IOVCC	-1	-	-	μA	2,3
VCSW High level leakage	ILIH2	Vin = 0 to VCI	-	-	1	μA	4
VCSW Low level leakage	ILIL2	Vin = 0 to VCI	-1	-	-	μA	4
Source OP Output							
Output deviation voltage	V_{dev}	Sout≧4.2V Sout≦0.8V			(TBD)	mV	
Output deviation voltage	V_{dev}	4.2V>Sout>0.8V			(TBD)	mV	
Output offset voltage	V_{OFSET}				(TBD)	mv	
Stand-by Current							
Sleep In mode	I_{stlp}	DSI LP mode IOVCC Current		(TBD)		uA	
		DSI LP mode VCI Current		(TBD)		uA	1
	I_{stul}	DSI Ultra Low power IOVCC Current		(TBD)		uA	
		DSI Ultra Low power VCI Current		(TBD)		uA	1

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit	Notes
Oscillator Output							
Oscillator tolerance	△OSC	Ta =25℃	-5%	-	5%	%	5

***Note* 1:** PCCS[1:0] pin =11 mode
***Note* 2:** Including of RESX ,PCCS[1:0], BS[2:0], TEST_OSC, BIST, DCX, CSX, SCL, TEST[2:0].
***Note* 3:** Including of CABC_PWM_OUT, TE, TE_TOUCH.
***Note* 4:** Including of VCSW1, VSCW2.
***Note* 5:** Oscillator frequency= 50MHz

4.3 MIPI characteristics

4.3.1 DC Characteristics for DSI LP Mode

Condition : Ta =25℃,IOVCC =1.6V~3.6V, VCI =2.6V~3.6V.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Logic high level input voltage	V_{IHLPCD}	LP-CD	450		1350	mV	
Logic Low level input voltage	V_{ILLPCD}	LP-CD	0		200	mV	
Logic high level input voltage	V_{IHLPRX}	LP-RX (CLK,D0)	880		1350	mV	
Logic Low level input voltage	V_{ILLPRX}	LP-RX (CLK,D0)	0		550	mV	
Logic Low level input voltage	$V_{ILLPRXULP}$	LP-RX(CLK ULP mode)	0		300	mV	
Logic high level input voltage	V_{OHLPTX}	LP-TX(D0)	1.1		1.3	V	
Logic Low level input voltage	V_{OLLPTX}	LP-TX(D0)	-50		50	mV	
Logic high level input voltage	I_{IH}	LP-RX,Vin =0~1.3V			10	uA	
Logic Low level input voltage	I_{IL}	LP-RX,Vin =0~1.3V	-10			uA	
Input pulse rejection	SGD	DSI-CLK+/-,DSI Dn+/-			300	Vps	1

***Note** 1: Peak interference amplitude max. 200mV and interference frequency min. 450MHz*

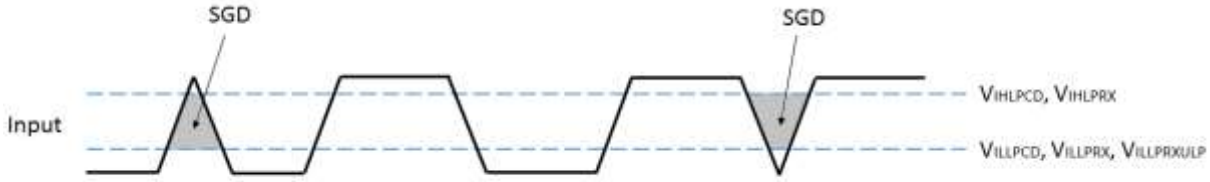


Figure 4-1 Spike/Glitch Rejection

4.3.2 DC Characteristics for DSI HS Mode

Condition : Ta =25℃,IOVCC =1.6V~3.6V, VCI =2.6V~3.6V.

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Input voltage common mode range	V_{CMCLK} V_{CMDATA}	CLK+/-, Dn+/-	70		330	mV	1,2
Input voltage common mode variation (≦450MHz)	$V_{CMRCLKL}$ $V_{CMRDATAL}$	CLK+/-, Dn+/-	-50		50	mV	3
Input voltage common mode variation (≧450MHz)	$V_{CMRCLKM}$ $V_{CMRDATAM}$	CLK+/-, Dn+/-			100	mV	
Low-level differential input voltage threshold	V_{THLCLK} $V_{THLDATA}$	CLK+/-, Dn+/-	-70			mV	
High-level differential input voltage threshold	V_{THHCLK} $V_{THHDATA}$	CLK+/-, Dn+/-			70	mV	
Single-ended input low voltage	V_{ILHS}	CLK+/-, Dn+/-	-40			mV	2
Single-ended input high voltage	V_{IHHS}	CLK+/-, Dn+/-			460	mV	2
Differential input termination resistor	R_{TERM}	CLK+/-, Dn+/-	80	100	125	Ω	
Single-ended threshold voltage for termination enable	V_{TERM_EN}	CLK+/-, Dn+/-			450	mV	
Termination capacitor	C_{TERM}	CLK+/-, Dn+/-			14	pF	

***Note** 1: Includes 50mV (-50mV to 50mV) ground difference*
***Note** 2: Without $V_{CMRCLKM}$ / $V_{CMRDATAM}$*
***Note**3: Without 50mV (-50mV to 50mV) ground difference*
***Note**4: Dn =D0,D1,D2 and D3*

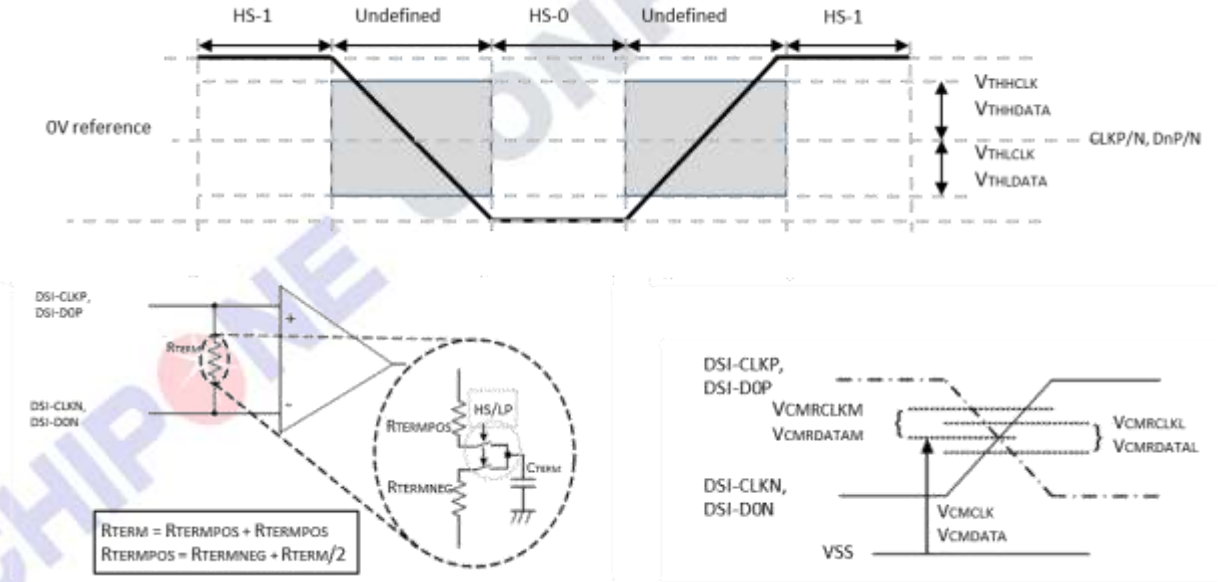


Figure 4-2 Differential voltage range, termination resistor and Common mode voltage

4.4 AC Timings Characteristics

4.4.1 Vertical Timings for DSI video mode

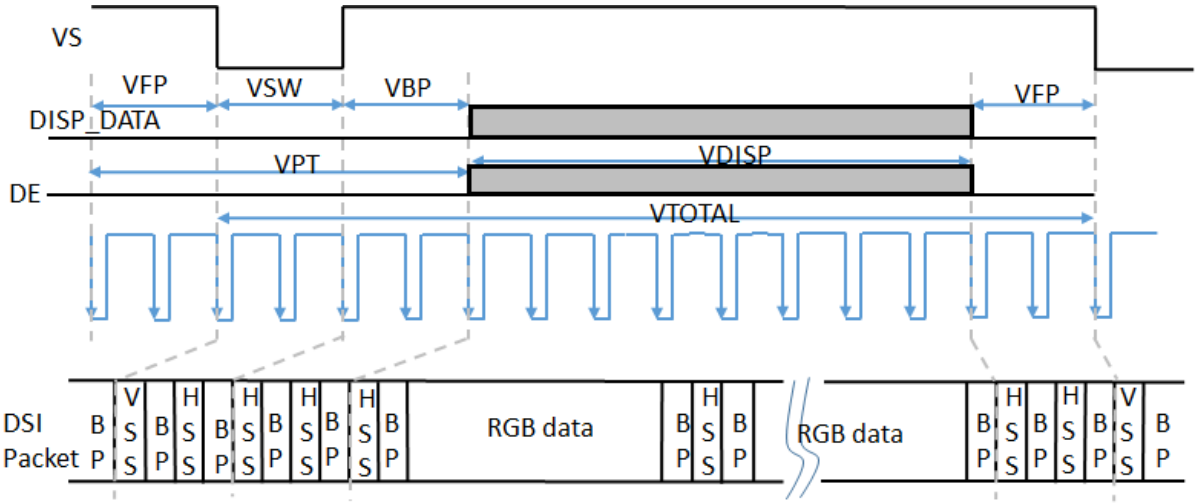


Figure 4-3 Vertical timings for DSI interface

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Vertical Total	V_{TOTAL}		(TBD)		(TBD)	Line	
Vertical low pulse width	VSW		(TBD)		(TBD)	Line	1
Vertical front porch	VFP		(TBD)		(TBD)	Line	
Vertical back porch	VBP		(TBD)		(TBD)	Line	1
Vertical data start point		VSW+VBP	(TBD)		(TBD)	Line	1
Vertical blanking period	VPT	VSW+VBP+VFP	(TBD)		(TBD)	Line	
Vertical active area		VDISP		1280	(TBD)	Line	
Vertical Frame rate	VFR			60		Hz	

Note 1: *The VSW and VBP pulse width are related to panel GOA timing. The GOA timing must be set at corresponding position for LCM normal display.*

4.4.2 Horizontal Timings for DSI video mode

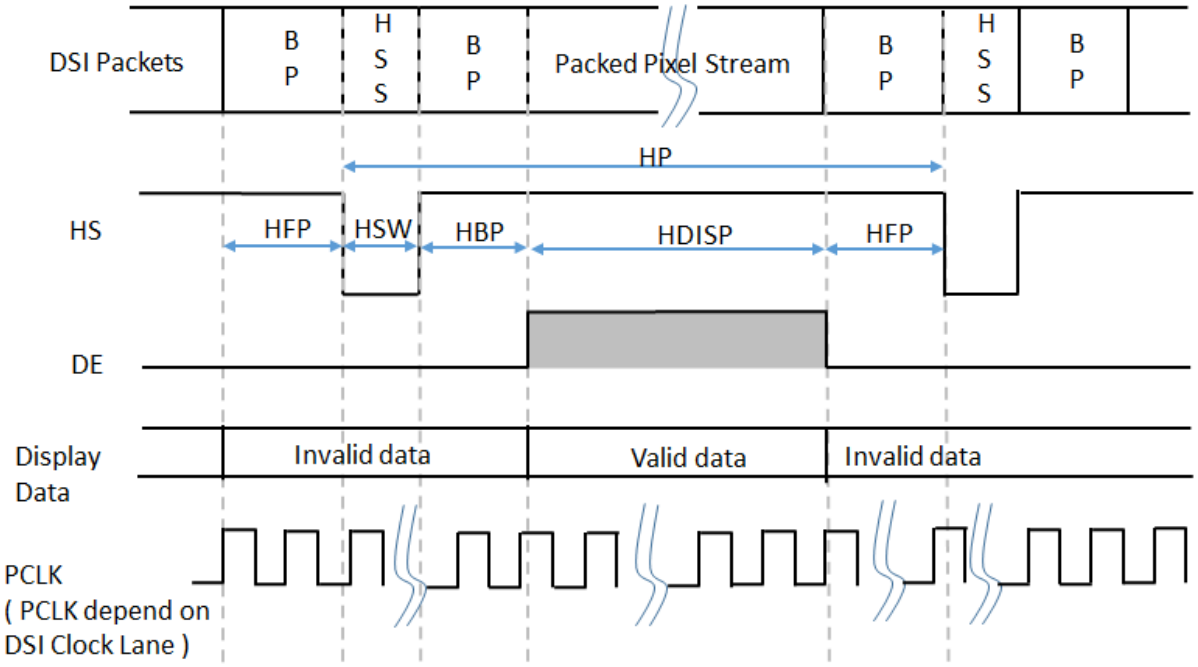


Figure 4-4 Horizontal timings for DSI video mode

Condition : Ta =25℃,Resolution = 720(RGB)*1280

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
HS low pulse width	HSW		(TBD)			uS	
Horizontal back porch	HBP		(TBD)			uS	
Horizontal front porch	HFP		(TBD)			uS	
Horizontal data start point		HSW+HBP	(TBD)			uS	
Horizontal blanking period	HBLK	HSW+HBP+HFP	(TBD)			uS	
Horizontal active area	HDISP			720		DCLK	

4.5 MIPI AC Characteristics

4.5.1 High Speed Mode - Clock Timings

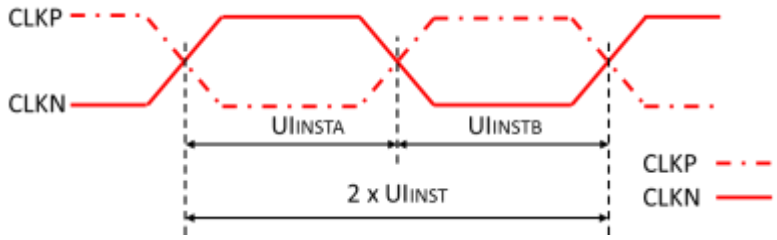


Figure 4-5 Clock Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CLK P/N	2xUIINST	Double UI instantaneous	4		18.2	nS	
CLK P/N	UIINSTA, UIINSTB	UI instantaneous Half	2		9.1	nS	1

***Note** 1*: UI = UIINSTA = UIINSTB

4.5.2 High Speed Mode - Clock / Data Timings

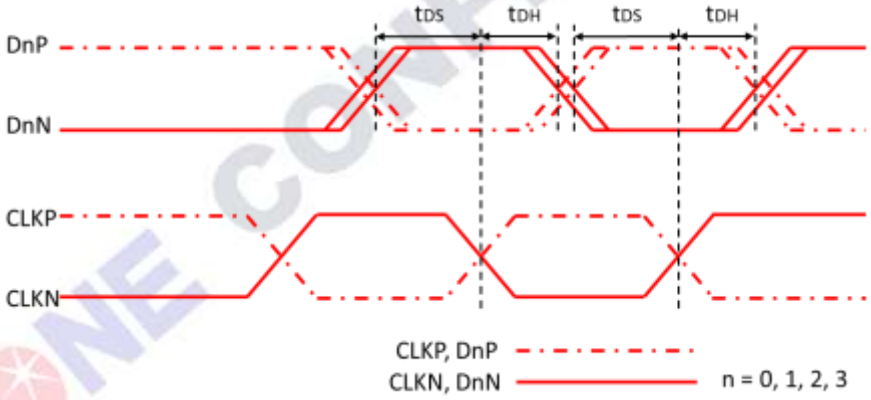


Figure 4-6 DSI Clock / Data Timings

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
Dn P/N (n=0,1,2 and 3)	tDS	Data to Clock Setup time	0.15*UI			UI	
	tDH	Clock to Data Hold time	0.15*UI			UI	

4.5.3 High Speed Mode - Rising and Falling Timings

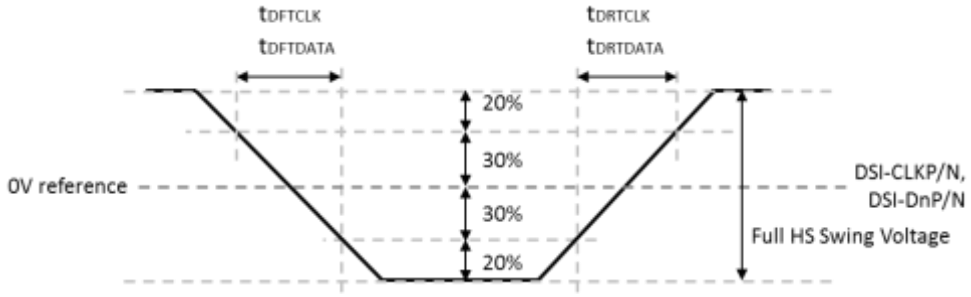


Figure 4-7 Rsing and Falling Timings

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Differential Rise Time for Clock	t_{DRTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Rise Time for Data	$t_{DRTDATA}$	DnP/N	150pS		0.3*UI		1,2,3
Differential Fall Time for Clock	t_{DFTCLK}	CLKP/N	150pS		0.3*UI		2,3
Differential Fall Time for Data	$t_{DFTDATA}$	DnP/N	150pS		0.3*UI		1,2,3

***Note* 1:** DnP/N, n =0,1,2 and 3

***Note* 2:** The display module has to meet timing requriements,which are defined for the transmitter (MCU) on MIPI D-PHY standard.

***Note* 3:** DSI-CLK+ = CLKP, DSI-CLK- =CLKN, DSI-D0+ =D0P, DSI-D0- =D0N

4.5.4 Low Speed Mode - Bus Turn Around

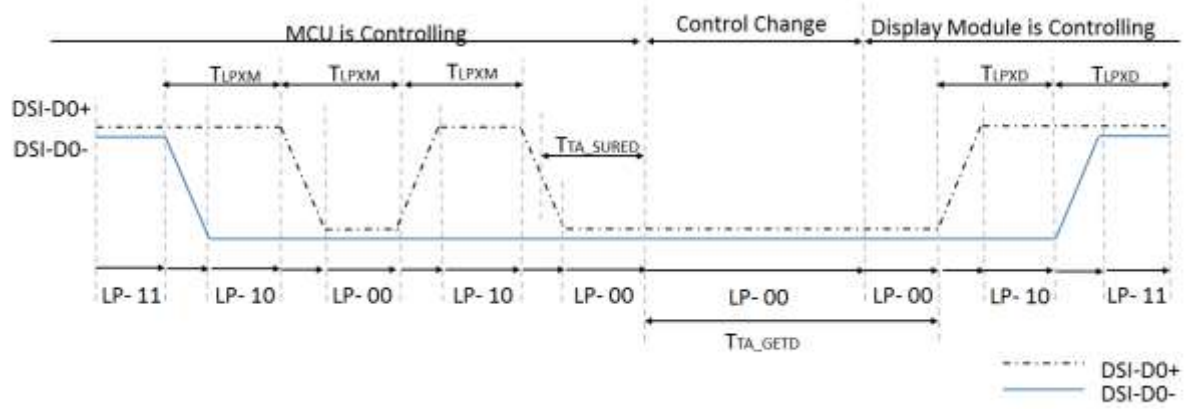


Figure 4-8 Bus Turnaround (BTA) from MCU to display module Timing

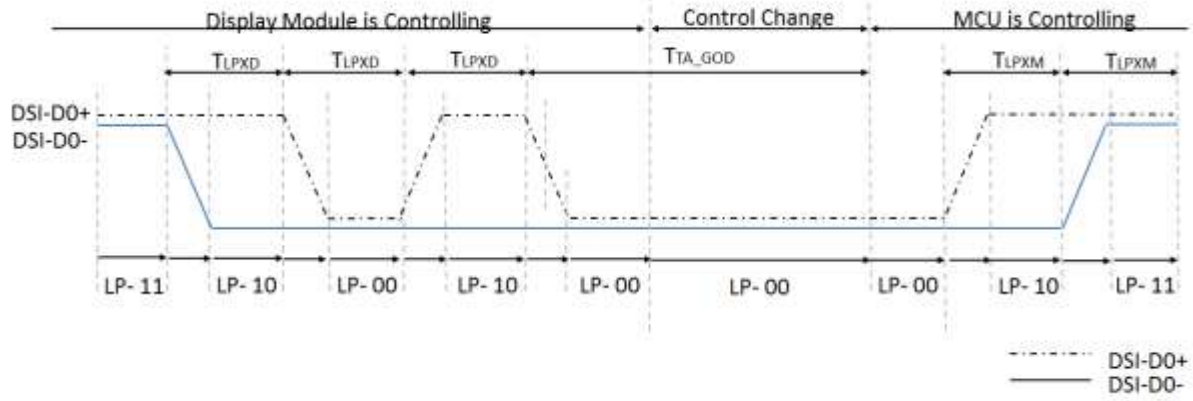


Figure 4-9 Bus Turnaround (BTA) from Display module to MCU Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
D0P/N	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP11 periods MCU to Display Module	50		75	nS	1
D0P/N	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP11 periods Display Module to MCU	50		75	nS	1
D0P/N	T_{TA_SURED}	Time-out before the Display Module starts driving	T_{LPXD}		2* T_{LPXD}	nS	1
D0P/N	T_{TA_GETD}	Time to drive LP-00 by Display Module	5* T_{LPXD}			nS	1
D0P/N	T_{TA_GOD}	Time to drive LP-00 after turnaround request -MCU	4 * T_{LPXD}			nS	1

Note 1: D0P = DSI-D0+, D0N = DSI-D0-

4.5.5 Data Lanes from Low Power Mode to High Speed Mode

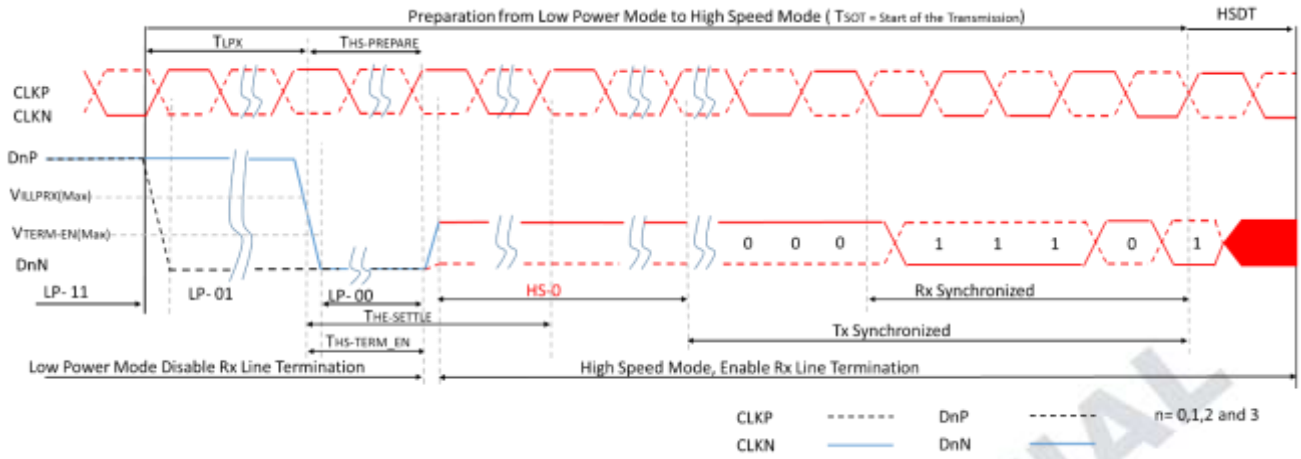
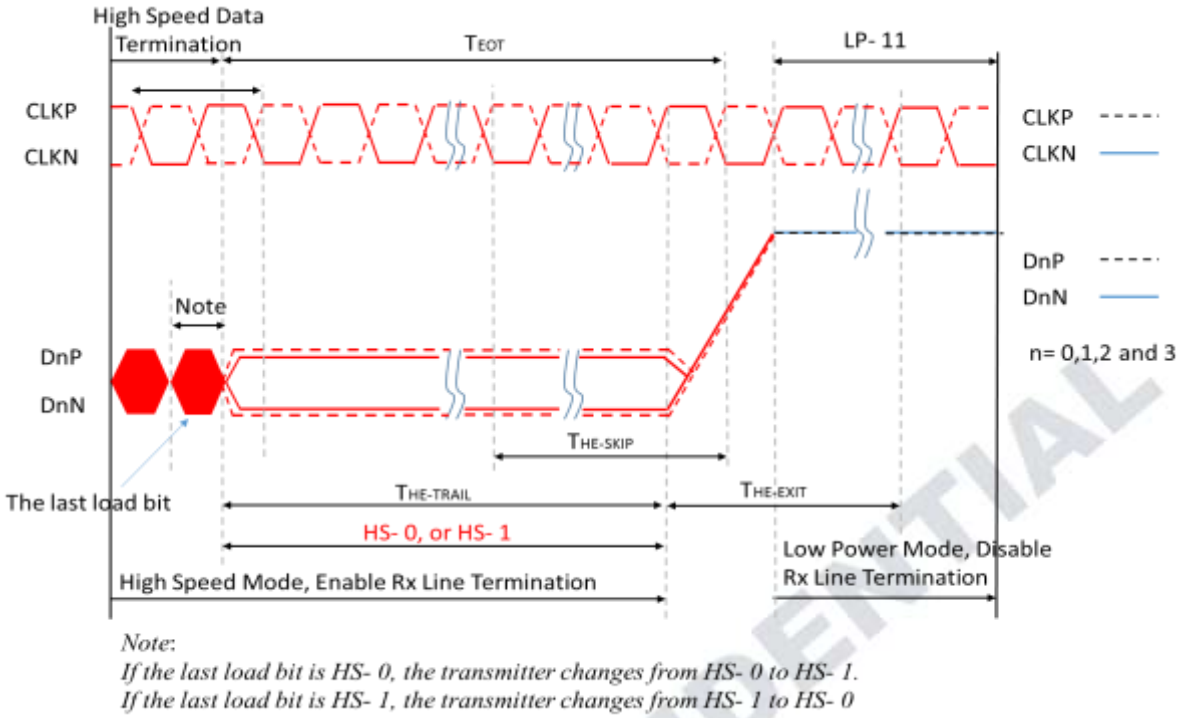


Figure 4-10 Data Lanes from Low Power Mode to High Speed Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	T_{LPX}	Length of any Low Power State Period	50			nS	1
DnP/N	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS Transmission	40+4*UI		85+6*UI	nS	1
DnP/N	$T_{HS-TREM-EN}$	Time to enable Data lane Receiver line termination measured from when Dn crosses VILMAX			35+4*UI	nS	1

Note 1: DnP/N, n=*0,1,2 and 3*

4.5.6 Data Lanes from High Speed Mode to Low Power Mode



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 4-11 Data Lanes from High Speed Mode to Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
DnP/N	THS-SKIP	Time-Out at Display Module to ignore transition period of EoT	40		55+4*UI	nS	1
DnP/N	THS-EXIT	Time to drive LP-11 after HS burst	100			nS	1

Note 1: DnP/N, n=*0,1,2 and 3*

4.5.7 DSI Clock Burst – High speed mode to /from Low Power Mode

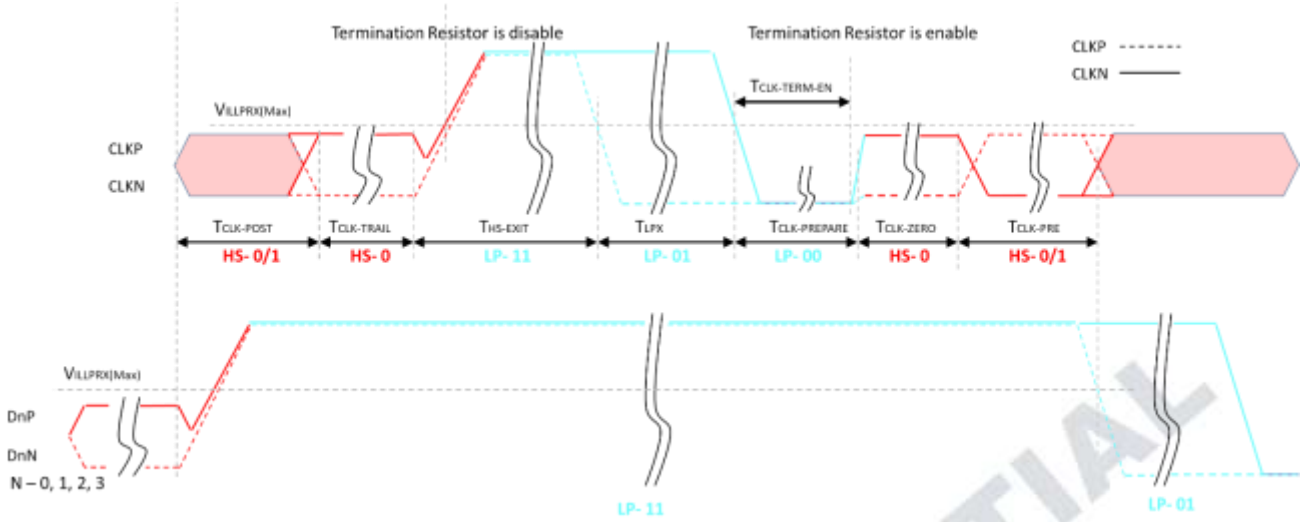


Figure 4-12 Clock Lane –High speed mode to / from Low Power Mode Timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
CKP/N	$T_{CK-POST}$	Time that the MCU shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52*UI			nS	
CKP/N	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60			nS	
CKP/N	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100			nS	
CKP/N	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38		95	nS	
CKP/N	$T_{CLK-TERM-EN}$	Time-out at Clock Lane to enable HS termination			38	nS	
CKP/N	$T_{CLK-PREPARE}$+ $T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting Clock	300			nS	
CKP/N	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8*UI			nS	

4.6 Reset Input Timing

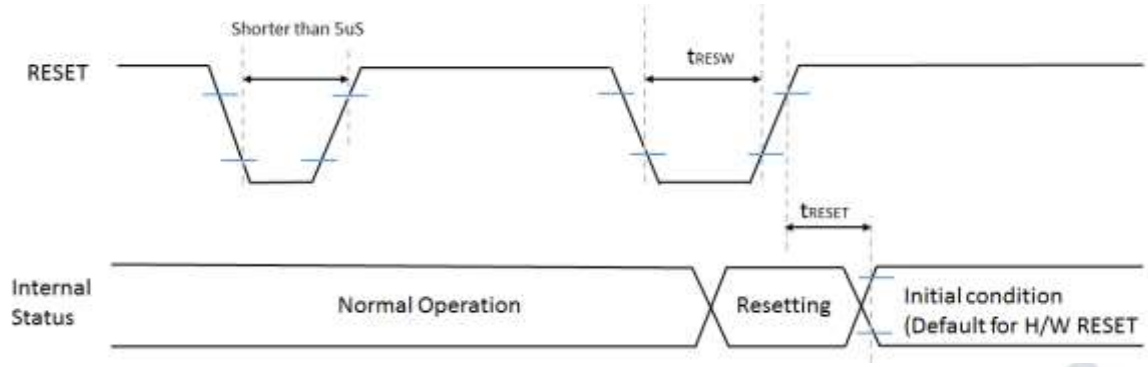


Figure 4-13 Reset Input Timing

Table 4-2 Reset Input Timing

Signal	Symbol	Parameter	Description	Specification			Unit	Notes
				MIN	TYP	MAX		
RESET	tRESW	Reset "L" pulse width		10			uS	1
	tRESET	Reset complete time	When reset applied during Sleep in mode			5	mS	2
			When reset applied during Sleep Out mode			120	mS	5

***Note* 1:** Condition : Ta =25℃

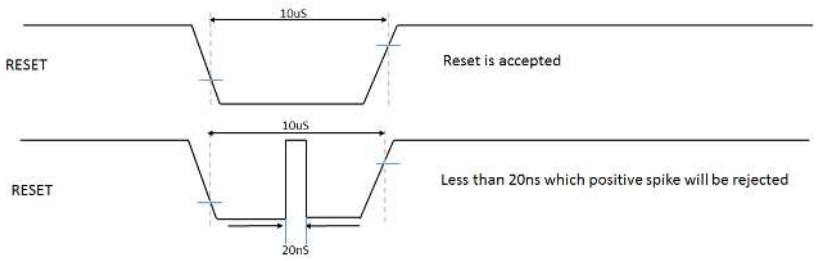
***Note* 2:** Spike due to an electrostatic discharge on RESET line does not cause irregular system reset according to the table below.

RESET Pulse	Action
Less than 5us	Reset Rejected
More than 10uS	Reset
Between 5us and 10uS	Reset Start

***Note* 2:** During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in sleep out mode. The display remains the blank state in sleep in mode) and then return to Default condition for H/W RESET.

Note3: During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W RESET complete time (tRESET) within 5ms after a rising edge of RESET.

***Note 4*:** Spike Rejection also applies during a valid reset pulse as shown below:



***Note 5*:** It is necessary to wait 5ms after releasing RESET when sending commands, and Sleep Out command can not be sent within 120ms.

5. Interface

5.1 Interface Level Communication

5.1.1 General

The display module uses data and clock lane differential pairs for DSI (DSI-1M). Both differential lane pairs can be driven to Low Power (LP) or High Speed (HS) mode.

Low Power mode means that each line of the differential pair is used in the single ended mode, a differential receiver is disable (a termination resistor of the receiver is disable), and it can be driven into a low power mode.

High Speed mode means that differential pairs (the termination resistor of the receiver is enable) are not used in the single ended mode.

Different modes and protocols are used in each mode when transferring information from the MCU to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low Power	
	DATA_P	DATA_N	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential - 0	Note1	Note1
HS-1	High (HS)	Low (HS)	Differential – 1	Note1	Note1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

***Note* 1:** Low-Power Receivers (LP-Rx) of the lane pair will check the LP-00 state code when the Lane Pair is in the High Speed (HS) mode.

***Note* 2 :** If Low-Power Receivers (LP-Rx) of the lane pair recognizes the LP-11 state code, then the lane pair will return to LP-11 of the Control Mode

***Note* 3:** n = 0, 1, 2 and 3 (D1P/N, D2 P/N and D3 P/N lanes only for HS-0 and HS-1)

5.1.2 DSI CLK Lanes

CLKP/N lanes can be driven into three different power modes: Low Power Mode (LPM), Ultra-Low Power Mode (ULPM) and High Speed Clock Mode (HSCM). Clock lane is in the single ended mode (LP = Low Power) when entering or leaving Low Power Mode (LPM) or Ultra-Low Power Mode (ULPM). Clock lane is in the single ended mode (LP = Low Power) when entering in or leaving High Speed Clock Mode (HSCM).These entering and leaving protocols use Clock lane in the single ended mode to generate an entering or leaving sequence. The principal flow chart of the different Clock lane power modes is illustrated below.

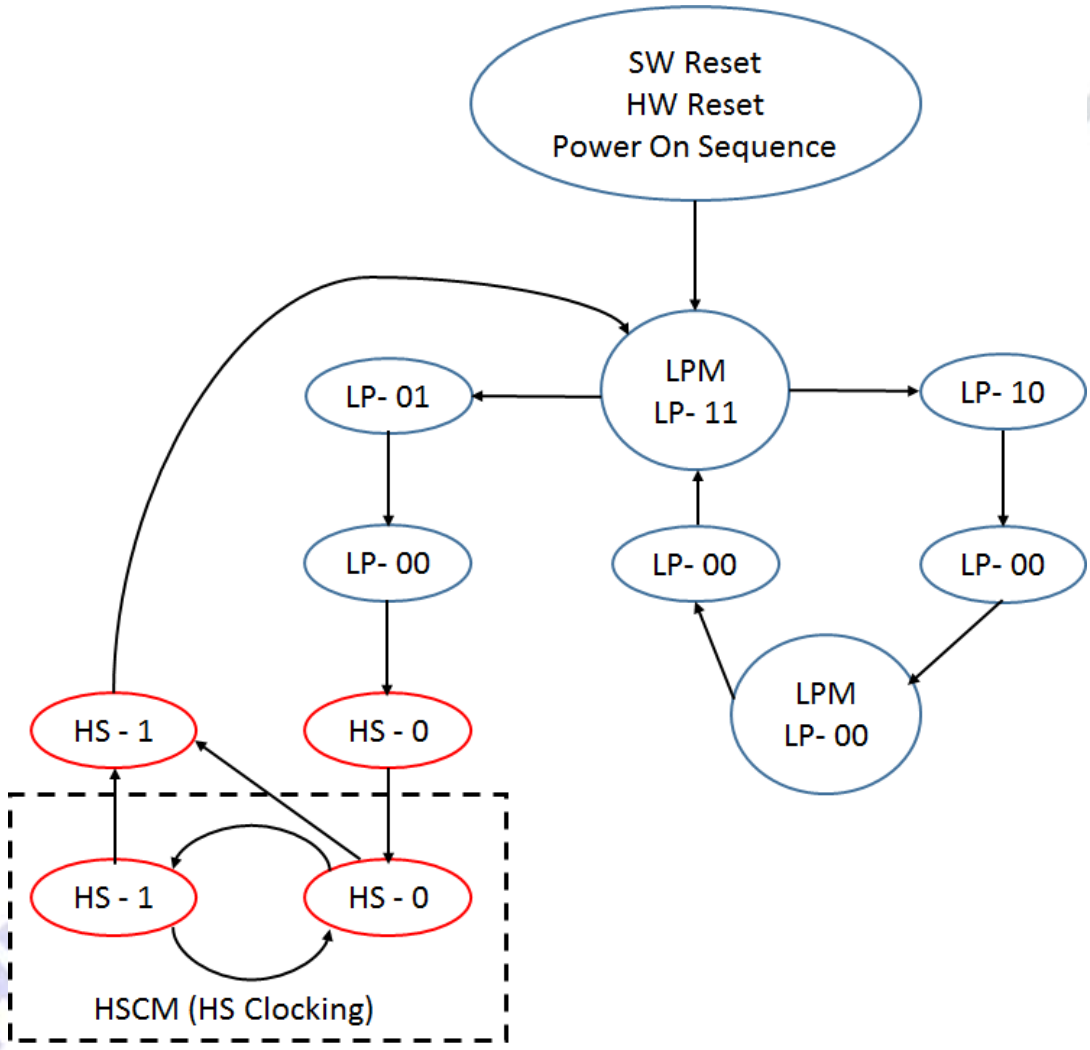


Figure 5-1 Clock Lane Power Modes

5.1.3 Low Power Mode (LPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11
2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

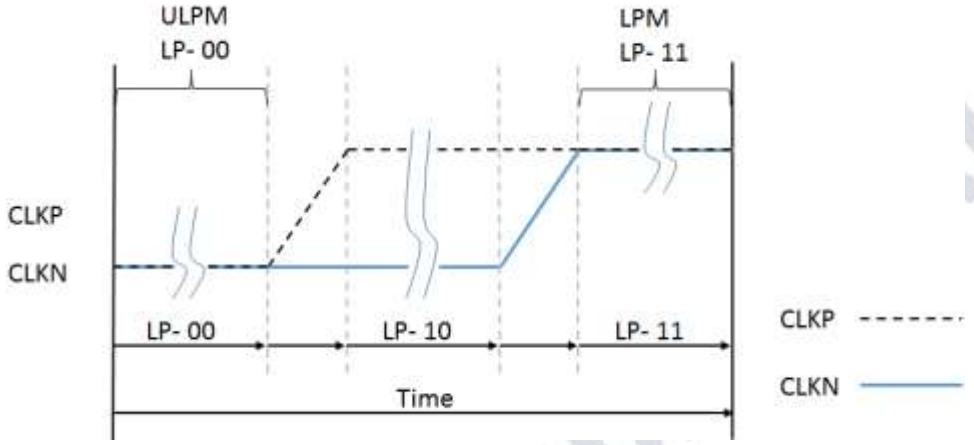


Figure 5-2 From ULPM to LPM

3) After CLKP/N lanes leave High Speed Clock Mode (HSCM, HS-0 or HS-1 State Code) => HS-0=> LP-11 (LPM).

This sequence is illustrated below.

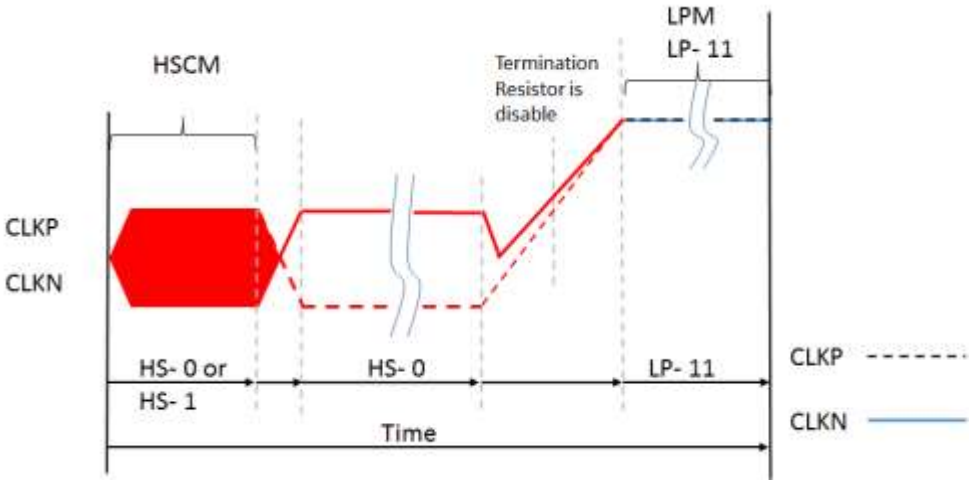


Figure 5-3 From High Speed Clock Mode (HSCM) to LPM

The changes of all the three modes are illustrated as below flow chart:

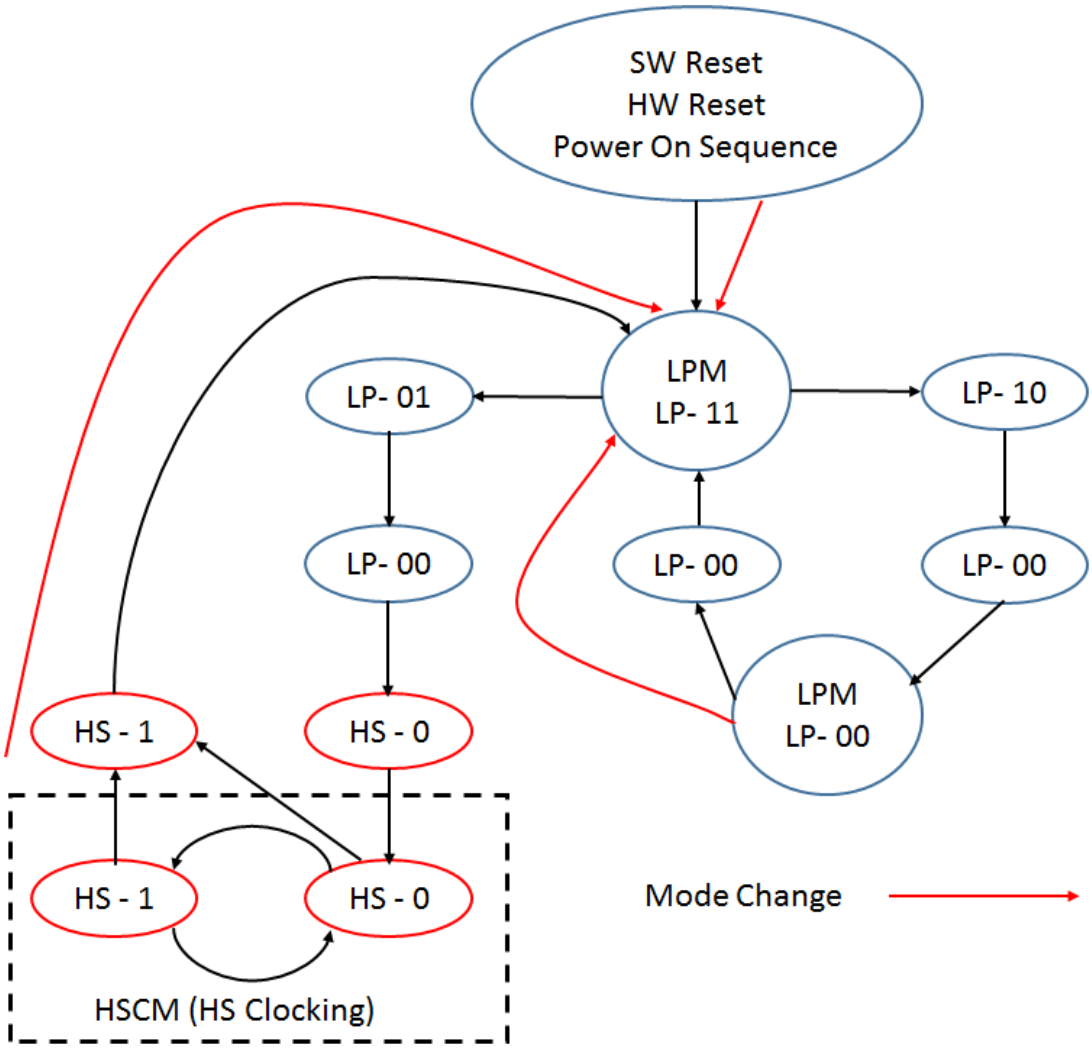


Figure 5-4 All Three Mode Changes to LPM

5.1.4 Ultra- Low Power Mode (ULPM)

CLKP/N lanes can be driven to the Low Power Mode (LPM), when CLKP/N lanes enter LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence => LP-11

2) After CLKP/N lanes leave Ultra-Low Power Mode (ULPM, LP-00 State Code) => LP-10 => LP-11 (LPM).

This sequence is illustrated below.

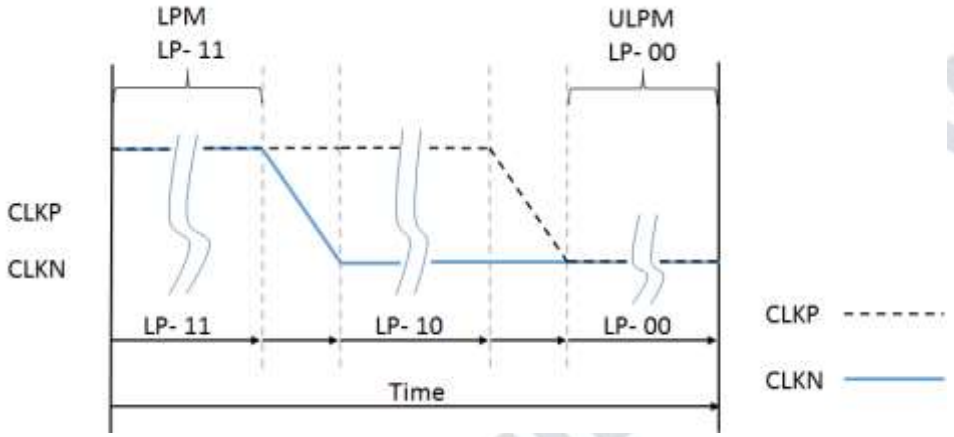


Figure 5-5 From LPM to ULPM

The mode change is also illustrated below.

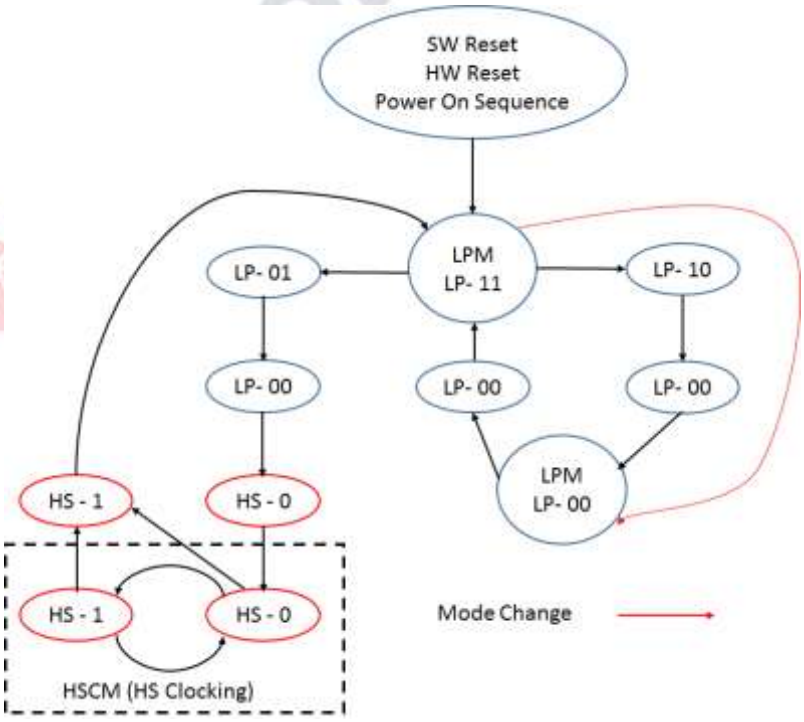


Figure 5-6 Mode Change from LPM to ULPM

5.1.5 High- Speed Clock Mode (HSCM)

CLKP/N lanes can be driven to the High Speed Clock Mode (HSCM) when CLK lanes start to function between HS-0 and HS-1 State Codes. The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) => LP-01 => LP-00 => HS-0 => HS-0/1 (HSCM). This sequence is illustrated below.

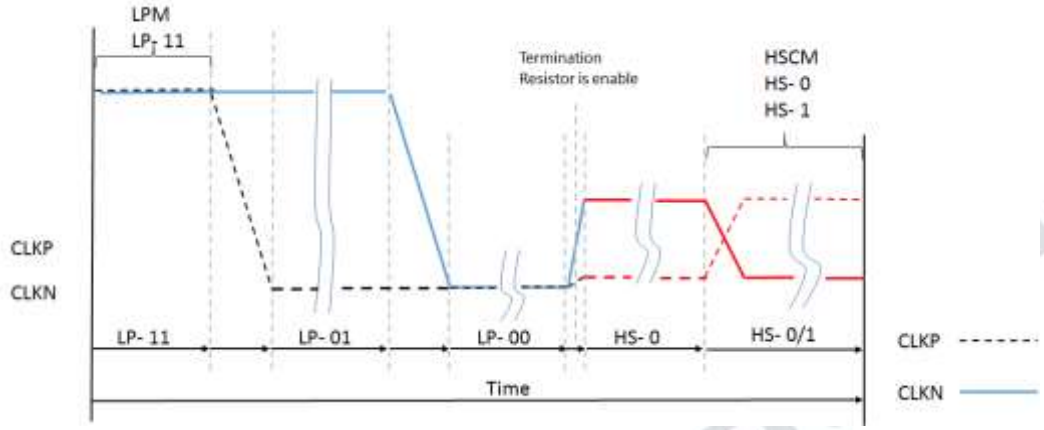


Figure 5-7 From LPM to HSCM

The mode change is also illustrated below.

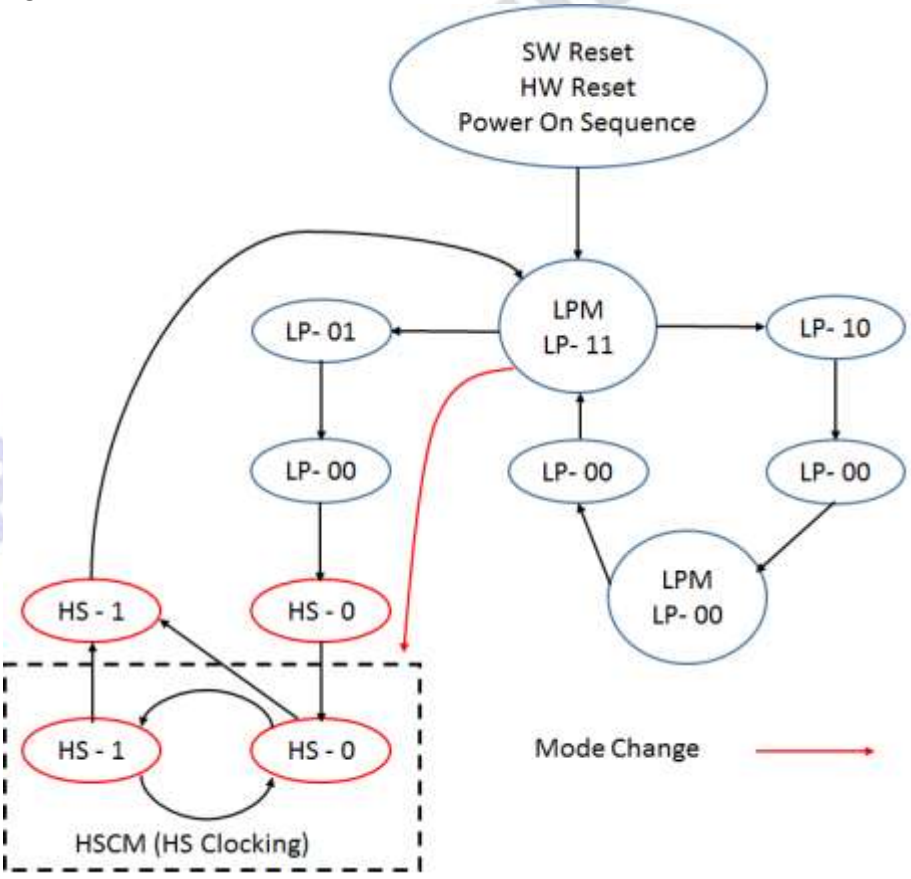
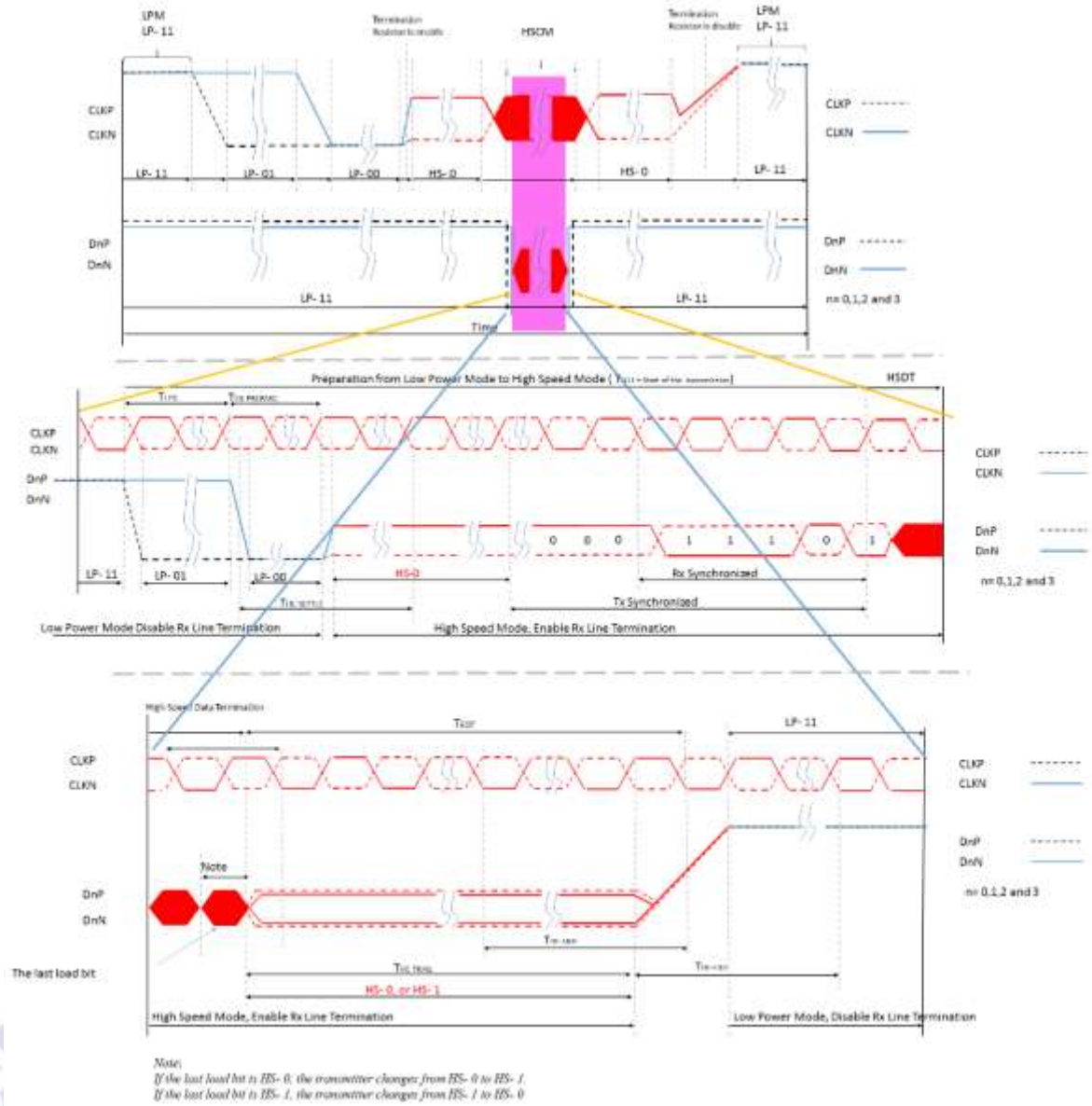


Figure 5-8 Mode Change from LPM to HSCM

The high speed clock (CLKP/N) starts before high speed data is sent via data lanes. The high speed clock continues clocking after the high speed data sending is stopped.

The burst of the high speed clock consists of:

- Even number of transitions
- Start state is HS- 0
- End state is HS- 0



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 5-9 High Speed Clock Burst

5.2 Interface Level Communication - DSI Data Lane

5.2.1 General

D3P/N, D2P/N, D1P/N, and D0P/N Data lanes can be driven into different modes:

- Escape Mode (Only D0P/N data lane is used)
- High- Speed Data Transmission (all data lanes are used)
- Bus Turnaround Request (Only D0P/N data lane are used)

These modes and their entering codes are defined in the following table.

Table 5-1

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP- 11→ LP- 10→ LP- 00 → LP- 01 → LP- 00	LP- 00→ LP- 10→ LP- 11 (Mark-1)
High- Speed Data Transmission	LP- 11→ LP- 01 → LP- 00 → HS- 0	(HS- 0 or HS- 1)→ LP11
Bus Turnaround Request	LP- 11→ LP- 10→ LP- 00 → LP- 10→ LP- 00	Hi- Z

5.2.2 Escape Modes

D0P/N data lanes can be used in different Escape Modes when data lanes are in the Low Power (LP) mode. These Escape Modes are used to:

- Send “Low-Power Data Transmission” (LPDT) from the MCU to the display module.
- Drive data lanes to “Ultra-Low Power State” (ULPS).
- Indicate “Remote Application Reset” (RAR), which can reset the display module.
  Indicate “Acknowledge” (ACK), which is used to transmit a non-error event from the display module to the MCU.

The basic sequence of the Escape Mode is as follows:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Escape Command (EC), which is coded, when one of the data lanes changes from low-to-high-to-low then this changed data lane presents the value of the current data bit (D0P = 1, D0N= 0). When DSI-D0 changes from low-to-high-to-low, the receiver will latch a data bit, which value is logical 0. The receiver will use this low-to-high-to-low transition as its internal clock.
- A load if it is needed
- Exit Escape (Mark-1) LP-00 => LP-10 => LP-11
- End: LP-11

This basic construction of Escape Modes is illustrated below:

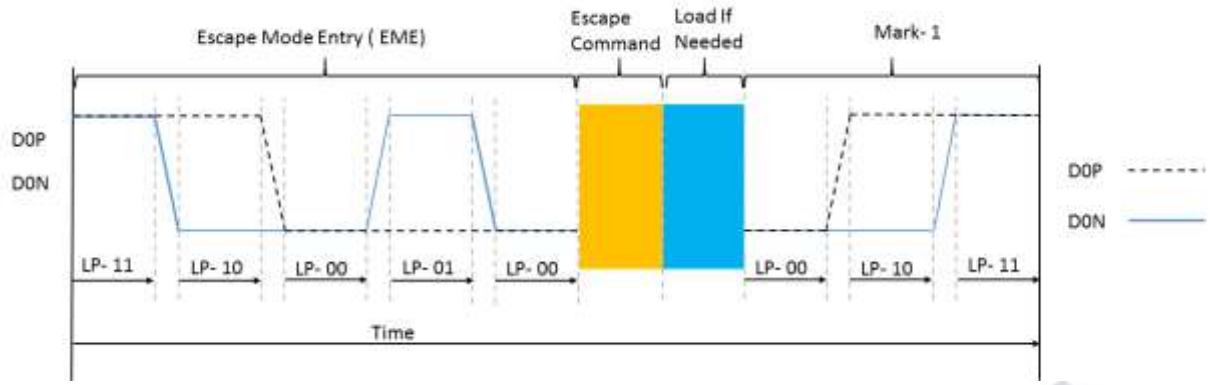


Figure 5-10 General Escape Mode Sequence

A total of eight Escape Commands (EC) are divided into two types: Mode and Trigger, as shown in below Table.

An example of the Mode type Escape Command is „Ultra-Low Power Mode", where the MCU instructs the display module to enter its Ultra-Low Power Mode.

Escape commands are defined in the following table.

Table 5-2 Escape mode command

Escape Command	Command Type Mode / Trigger	Entry command Pattern (First Bit→ Last Bit Transmitted)	Dn	D0
Low- Power Data Transmission	Mode	1110 0001 bin		x
Ultra- Low Power Mode	Mode	0001 1110 bin	x	x
Underfined- 1, Note1	Mode	1001 1111 bin		
Underfined- 2, Note1	Mode	1101 1110 bin		
Remote Application Reset	Trigger	0110 0010 bin		x
Acknowledge	Trigger	0010 0001 bin		x
UnKnow- 5, Note1	Trigger	1010 0000 bin		

***Note* 1:** This Escape command support is not implemented on the display module.

***Note* 2:** n=1

***Note* 3:** x= supported

5.2.3 Low- Power Data Transmission (LPDT)

The MCU can send data to the display module in the Low-Power Data Transmission (LPDT) mode when data lanes enter the Escape Mode and Low-Power Data Transmission (LPDT) command is sent to the display module.
The display module also uses the same sequence when it sends data to the MCU. The Low Power Data
Transmission (LPDT) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Low-Power Data Transmission (LPDT) command in the Escape Mode: 1110 0001 (first to last bit)
- Load (Data):
- One or more bytes (one byte = 8 bit)
- Data lanes are in pause mode when data lanes are stopped (both lanes are low) between bytes
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

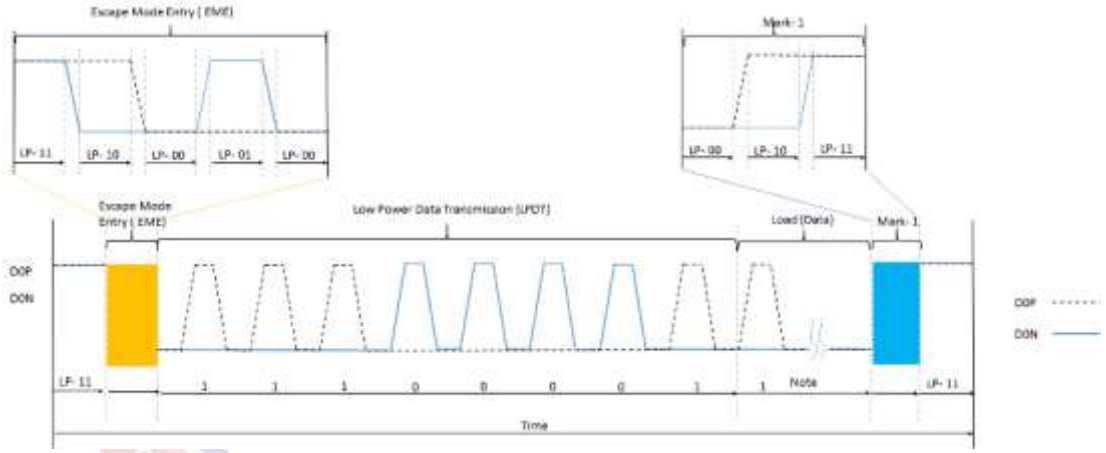


Figure 5-11 Low- Power Data Transmission (LPDT)

***Note**:* Load (Data) presents that the first bit is the logical 1 in this example.

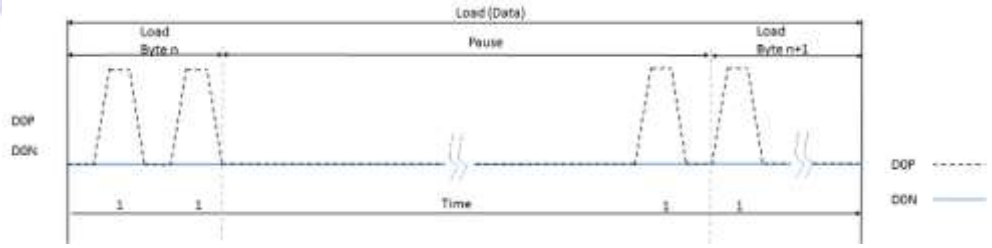


Figure 5-12 Pause (Example)

5.2.4 Ultra- Low Power State (ULPS)

The MCU can force data lanes get into the Ultra-Low Power State (ULPS) mode when data lanes enter the Escape Mode. The Ultra-Low Power State (ULPS) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Ultra-Low Power State (ULPS) command in the Escape Mode: 0001 1110 (first to last bit)
- Ultra-Low Power State (ULPS) when the MCU keeps data lanes low
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11 (Next command must wait 100us after data lanes leave ULPS)

This sequence is illustrated for reference purposes below:

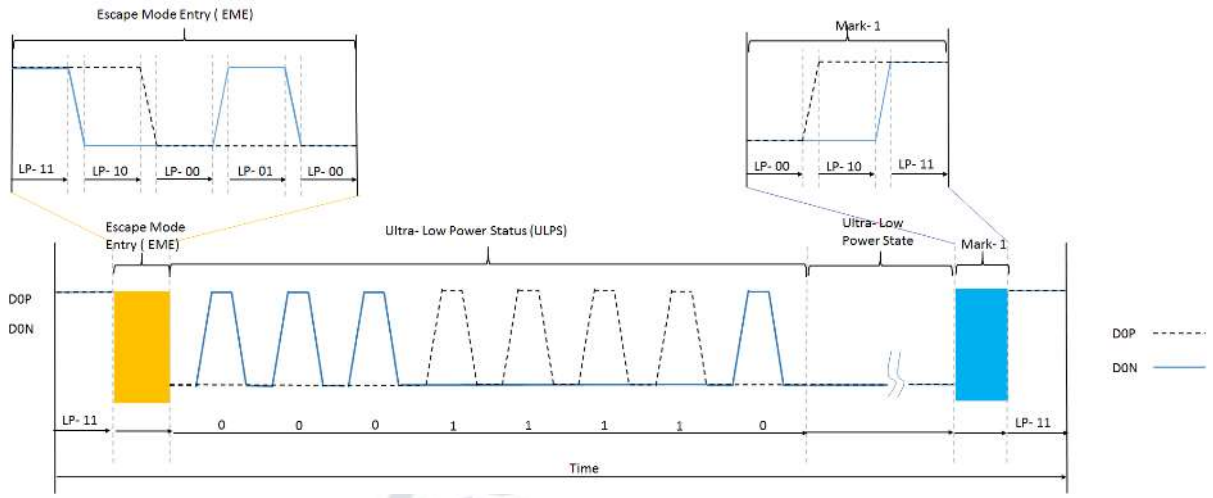


Figure 5-13 Ultra- Low Power State (ULPS)

5.2.5 Remote Application Reset (RAR)

The MCU can inform the display module that it should be reset in Remote Application Reset (RAR) trigger when data lanes enter the Escape Mode. The Remote Application Reset (RAR) uses the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

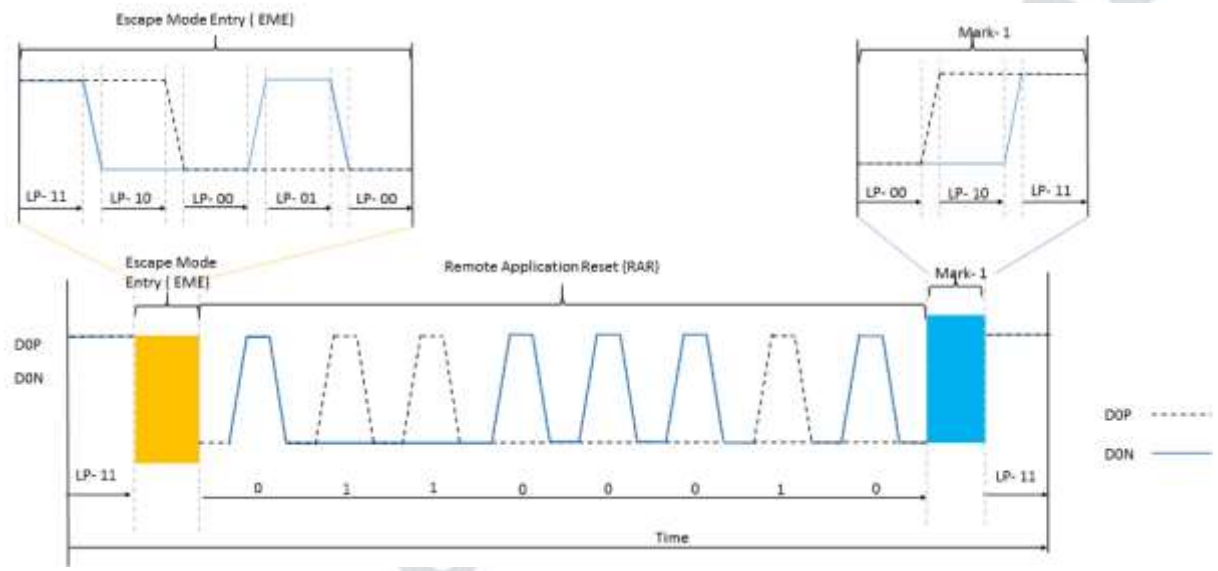


Figure 5-14 Remote Application Reset (RAR)

5.2.6 Acknowledge (ACK)

The display module can inform the MCU an error is not recognized by Acknowledge (ACK). The display module sends the Acknowledge (ACK) with the following sequence:

- Start: LP-11
- Escape Mode Entry (EME): LP-11 => LP-10 => LP-00 => LP-01 => LP-00
- Acknowledge (ACK) command in the Escape Mode: 0010 0001 (first to last bit)
- Mark-1: LP-00 => LP-10 => LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

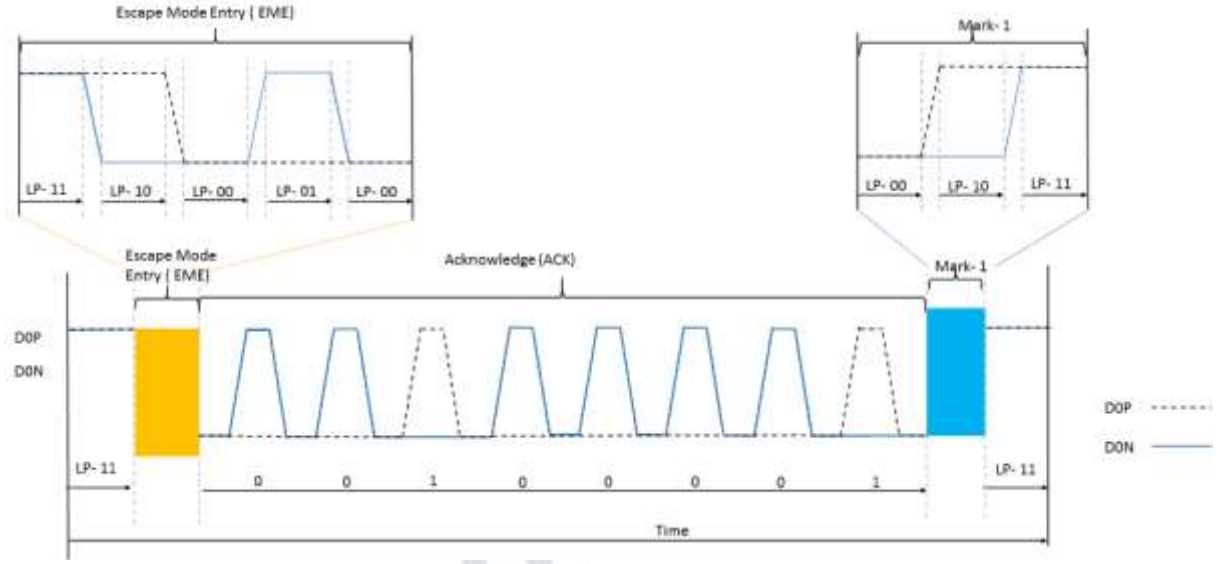


Figure 5-15 Acknowledge (ACK)

5.2.7 Entering High- Speed Data Transmission (TSOT of HSDT)

The display module enters High-Speed Data Transmission (HSDT) when Clock lane CLKP/N have already entered the High-Speed Clock Mode (HSCM) by the MCU. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module enter the High-Speed Data Transmission (TSOT of HSDT) as follows:

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= MCU) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

The sequence of entering High-Speed Data Transmission (TSOT of HSDT) is illustrated below:

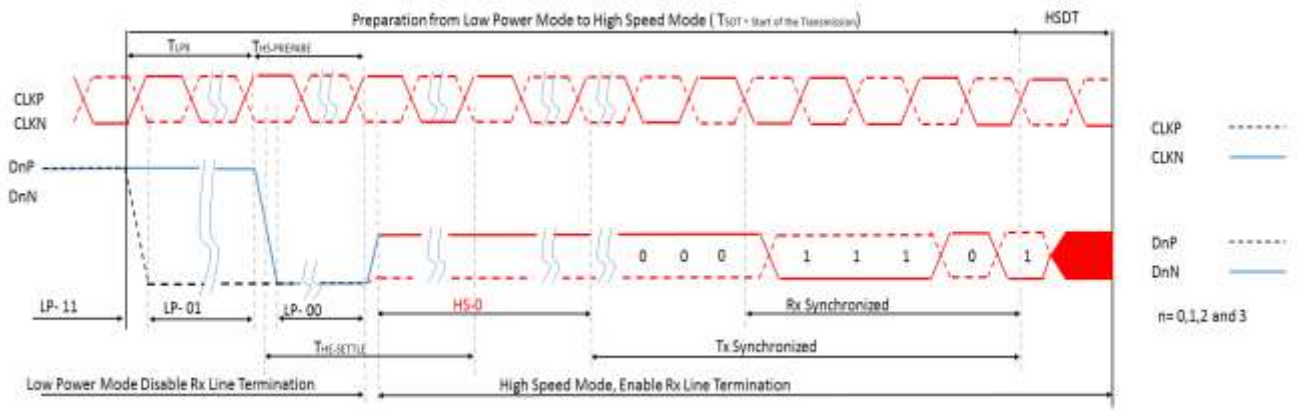


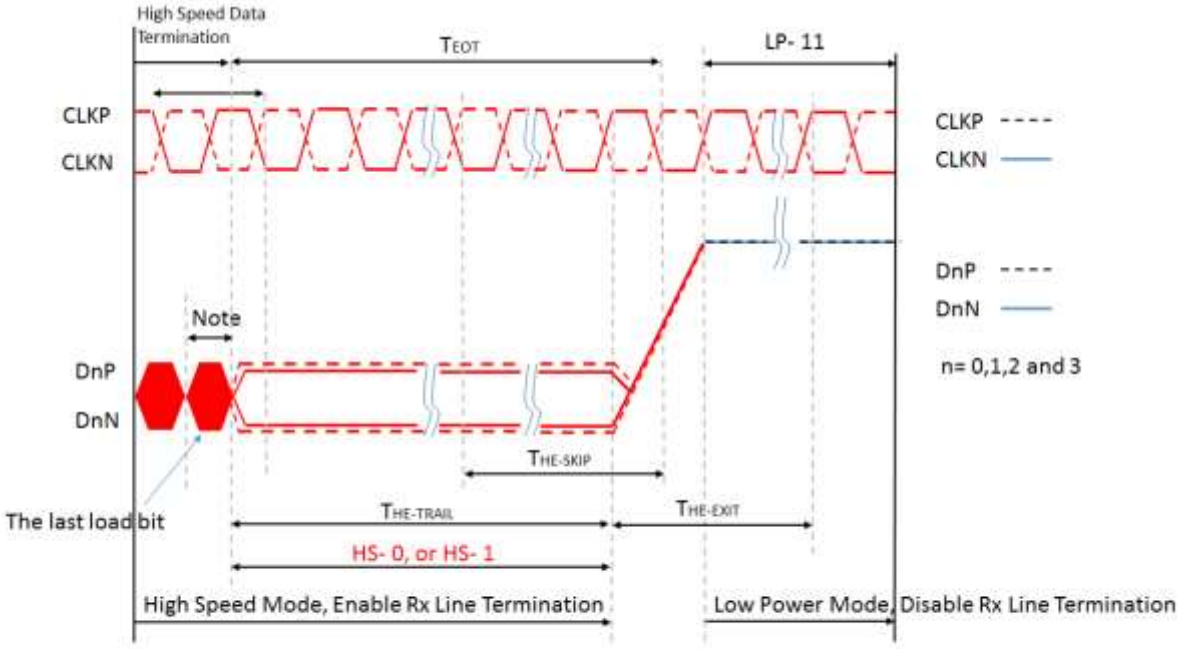
Figure 5-16 Entering High- Speed Data Transmission (TSOT of HSDT)

5.2.8 Leaving High- Speed Data Transmission (TEOP of HSDT)

The display module leaves the High-Speed Data Transmission (TEOT of HSDT) when Clock lane DSICLK+/- are in the High-Speed Clock Mode (HSCM) by the MCU, and this HSCM is kept until data lanes D3P/N, D2P/N, D1P/N and D0P/N are in the LP-11 mode. See more information in the section “High-Speed Clock Mode (HSCM)”. Data lanes D3P/N, D2P/N, D1P/N and D0P/N of the display module leave the High-Speed Data Transmission (TEOT of HSDT) as follows:

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- MCU changes to HS-1, if the last load bit is HS-0
- MCU changes to HS-0, if the last load bit is HS-1
- End: LP-11 (Rx: Lane Termination Disable)

The sequence of leaving High-Speed Data Transmission (TEOT of HSDT) is illustrated below:



Note:
If the last load bit is HS- 0, the transmitter changes from HS- 0 to HS- 1.
If the last load bit is HS- 1, the transmitter changes from HS- 1 to HS- 0

Figure 5-17 Leaving High- Speed Data Transmission (TEOT of HSDT)

5.2.9 Burst of the High- Speed Data Transmission (HSDT)

The burst of the “High-Speed Data Transmission” (HSDT) can consist of one or several data packet(s). These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined in the section “Short Packet (SPa) and Long Packet (LPa) Structures”. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

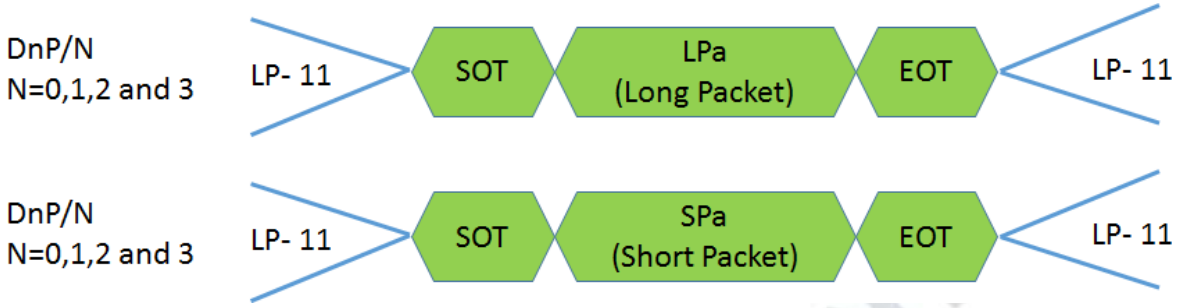


Figure 5-18 Single Packet in High- Speed Data Transmissions

The multiple packets in High-Speed Data Transmission are illustrated for reference purposes below:

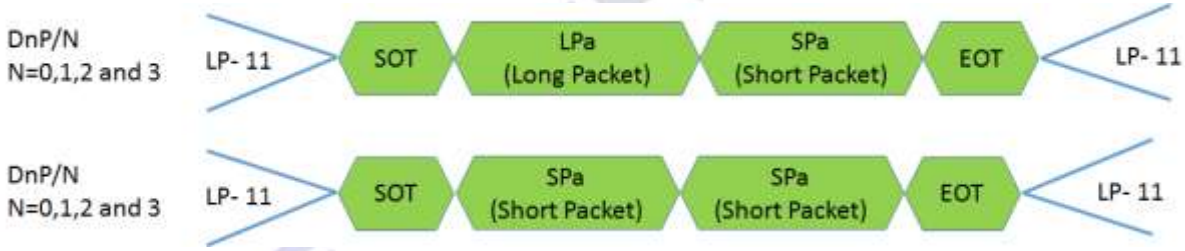


Figure 5-19 Multiple Packets in High- Speed Data Transmission – Example

Abbreviation	Explanation
EOT	End of the Transmission
LPa	Long Packet
LP-11	Low Power Mode, Both of Data lanes are “1”s (Stop Mode)
SPa	Short Packet
SOT	Start of the Transmission

5.2.10 Bus Turnaround (BTA)

The MCU or display module, which controls D0P/N Data Lanes, can start a bus turnaround procedure when it requires information from a receiver, which can be the MCU or display module. The MCU and display module use the same sequence when this bus turnaround procedure is used. The sequence, when the MCU wants to do the bus turnaround procedure to the display module, is described for reference purposes as follows:

- Start (MCU): LP-11
- Turnaround Request (MCU): LP-11 => LP-10 => LP-00 => LP-10 => LP-00
- The MCU waits until the display module starts to control D0P/N data lanes and the MCU stops to control D0P/N data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 => LP-10 => LP-11

The bus turnaround procedure (from the MCU to the display module) is illustrated below:

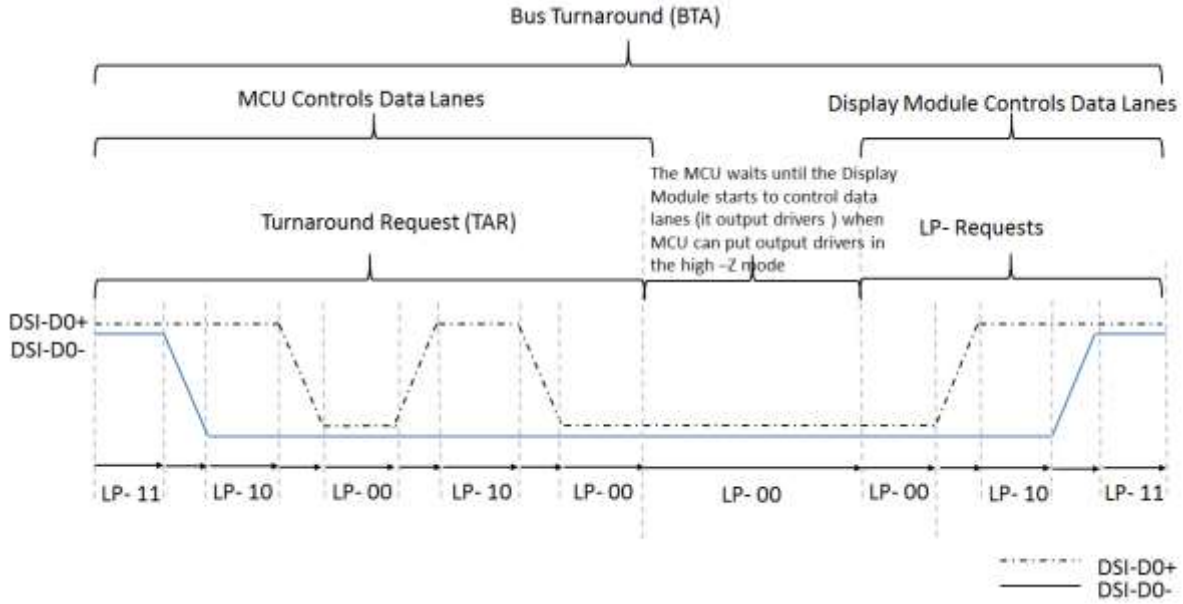


Figure 5-20 Bus Turnaround Procedure

MCU and display module terms can be switched as Figure 5-20 Bus Turnaround Procedure when the Bus Turnaround (BTA) is from the display module to the MCU.

5.3 Packet Level Communication

5.3.1 Short Packet (SPa) and Long Packet (LPa) Structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSDT) modes. The lengths of the packets are:

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

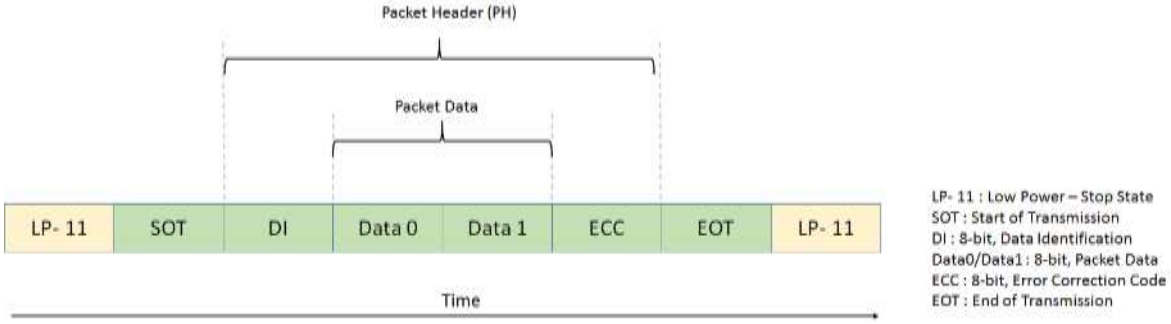


Figure 5-21 Short Packet (SPa) Structure

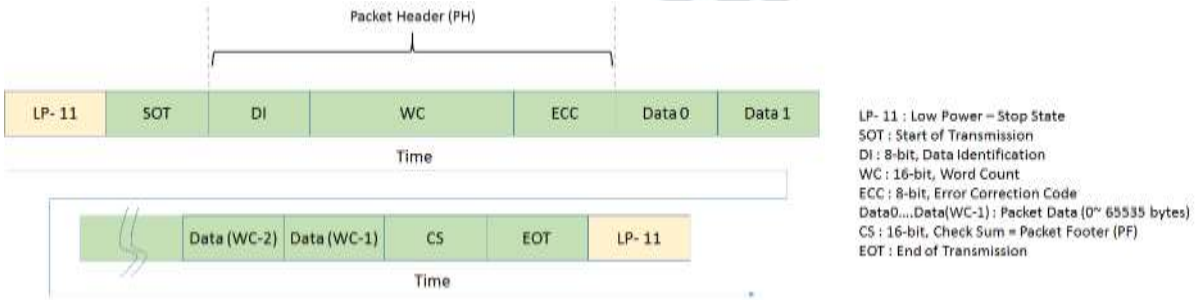


Figure 5-22 Long Packet (LPa) Structure

Notes:

1. Figure 5.4.1-1 and 5.4.1-2 present a single packet sending (= Includes LP-11, SOT and EOT for each packet sending).
2. The other possibility is that SOT, EOT and LP-11 are not needed between packets if packets are sent in multiple packet format, e.g:

- LP-11 → SOT → SPa → LPa → SPa → SPa → EOT → LP-11
- LP-11 → SOT → SPa → SPa → SPa → EOT → LP-11
- LP-11 → SOT → LPa → LPa → LPa → EOT → LP-11

5.3.2 Bit Order of the Byte on Packet

The bit order of the byte, what is used in packets, is that the Least Significant Bit (LSB) of the byte is sent first, and the Most Significant Bit (MSB) is sent last. The order is illustrated for reference purposes below.

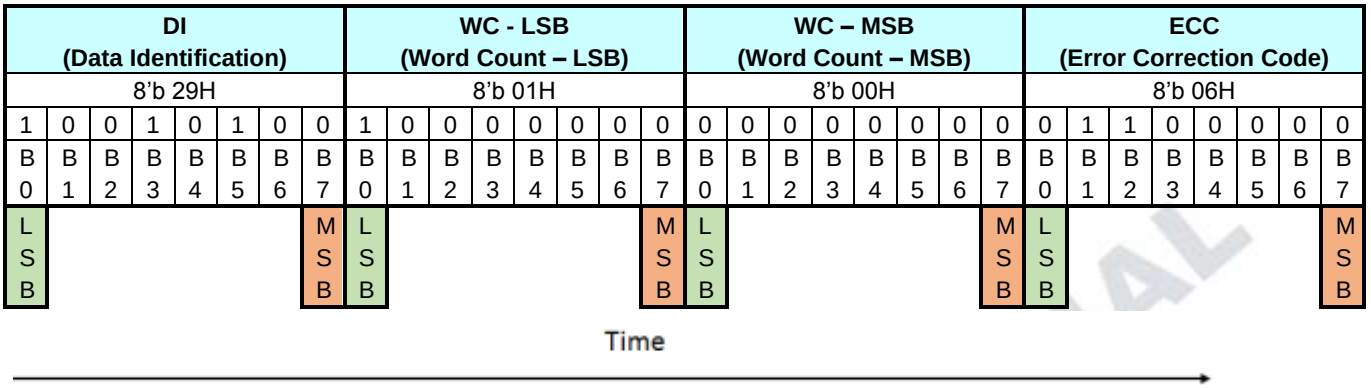


Figure 5-23 Bit order of the byte on packet

5.3.3 Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used in packets, is that the Least Significant (LS) Byte of the information is sent first and the Most Significant (MS) Byte is sent last. For example, Word Count (WC) consists of 2 bytes (= 16 bits); while the LS byte is sent first and the MS byte is sent last. The order is illustrated for reference purposes below.

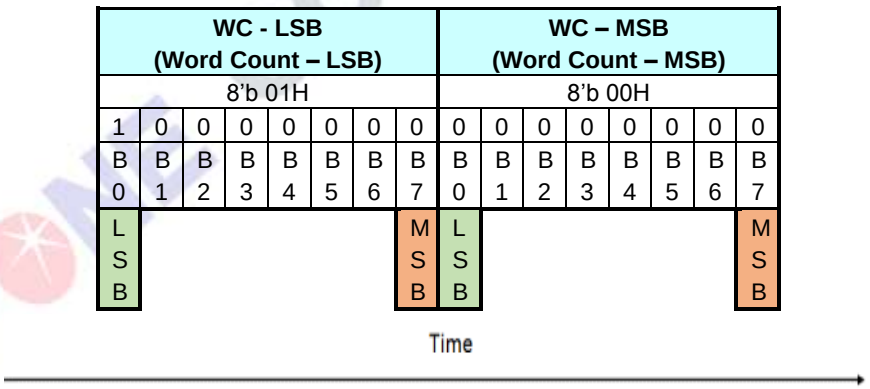


Figure 5-24 Byte order of the multiple byte information on packets

5.3.4 Packet Header (PH)

The packet header always consists of 4 bytes. The content of these 4 bytes are different for Short Packet (SPa) and Long Packet (LPa).

➢ Short Packet (SPa)

- 1st byte: Data Identification (DI) => Identify that this is a Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 3AH								8'b 07H								8'b 18H							
1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-25 Packet Header (PH) in a Short Packet (SPa)

➢ Long Packet (LPa)

- 1st byte: Data Identification (DI) => Identify that this is a Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-26 Packet Header (PH) in a Long Packet (LPa)

5.3.5 Data Identification (DI)

Data Identification (DI) is a part of the Packet Header (PH), and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI [7...6]
- Data Type (DT), 6 bits, DI [5…0]

The Data Identification (DI) structure is illustrated, see the figure below.

DI (Data Identification)							
VC (Virtual Channel Identifier)		DT (Data Type)					
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

Figure 5-27 Data Identification (DI) Structure

Data Identification (DI) in the Packet Header (PH) is illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 29H								8’b 01H								8’b 00H								8’b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-28 Data Identification (DI) on the Packet Header (PH)

5.3.6 Virtual Channel (VC)

Virtual Channel (VC) is a part of Data Identification (DI [7:6]) structure, and it is used to address where a packet is to be sent from the MCU. Bits of the Virtual Channel (VC) are illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-29 Virtual Channel (VC) on the Packet Header (PH)

Virtual Channel (VC) can assign 4 different channels for 4 different display modules. Devices will use the same virtual channel as which the MCU uses to send packets to them, e.g.

- The MCU uses the virtual channel 0 when it sends packets to the ICNL9707.
- The ICNL9707 also uses the virtual channel 0 when it sends packets to the MCU

This functionality is illustrated below.

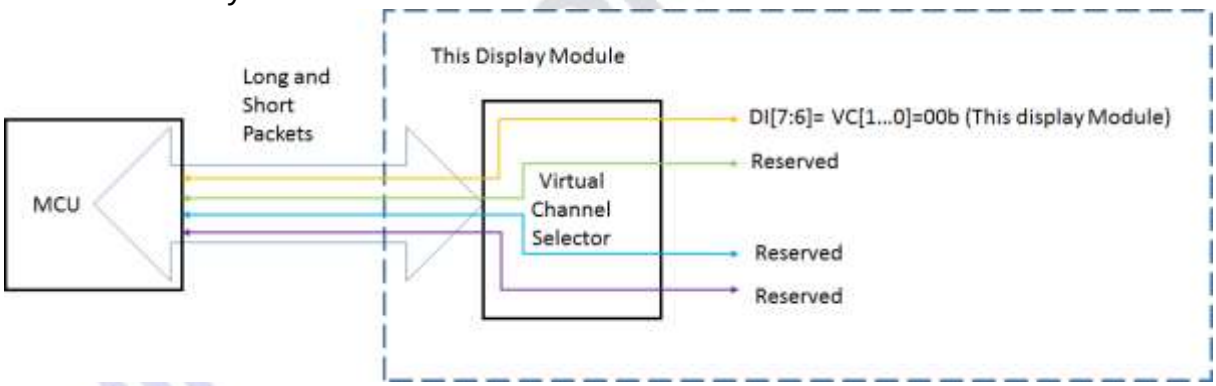


Figure 5-30 Virtual channel diagram

Virtual Channel (VC) is always 0 (DI [7:6] = VC [1:0] = 00b) when the MCU sends "End of Transmission Packet" to the display module. See the section "End of Transmission Packet (EoTP)". This display module does not support the virtual channel selector for other devices (1 to 3) when the only possible virtual channel (VC [1:0]) is 00b for the ICNL9707.

5.3.7 Data Type (DT)

Data Type (DT) is a part of Data Identification (DI [5…0]) structure, and it is used to define the type of the used data in a packet. Bits of the Data Type (DT) are illustrated for reference purposes below.

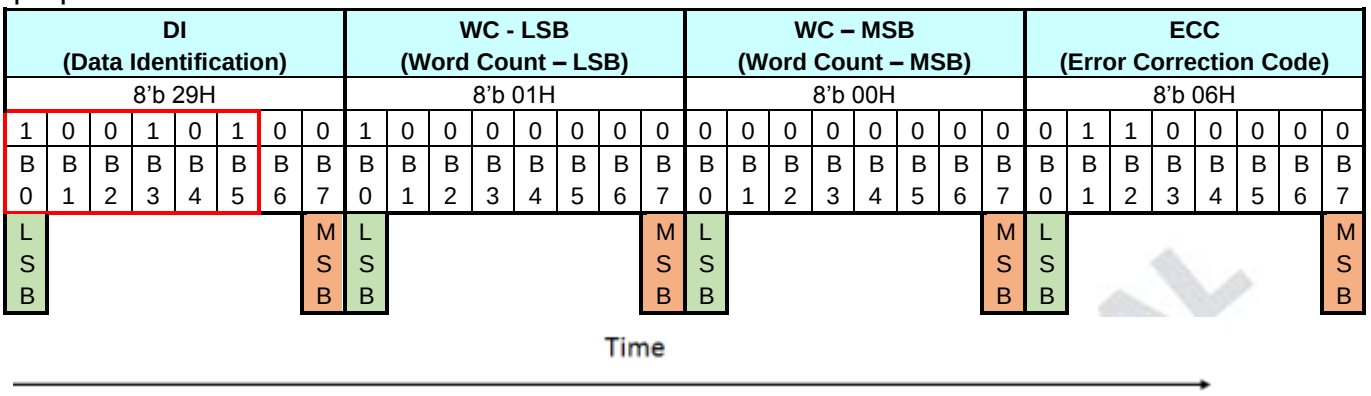


Figure 5-31 Data Type (DT) on the Packet Header (PH)

This Data Type (DT) also defines the used packet is a Short Packet (SPa) or a Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Types (DT) are defined in the tables below.

Table 5-3 Data type from the TX to RX

From the MCU to the Display Module		
Hex	Description	Short / Long Packet
01	Sync Even, V Sync Start	SPa (Short Packet)
11	Sync Even, V Sync End	SPa (Short Packet)
21	Sync Even, H Sync Start	SPa (Short Packet)
31	Sync Even, H Sync End	SPa (Short Packet)
08	End of Transmission Packet (EOTP) Note1	SPa (Short Packet)
02	Color Mode Off Command	SPa (Short Packet)
12	Color Mode On Command	SPa (Short Packet)
22	Shut Down Peripheral Command	SPa (Short Packet)
32	Turn On Peripheral Command	SPa (Short Packet)
03	Generic Short WRITE, no parameters	SPa (Short Packet)
13	Generic Short WRITE, 1 parameters	SPa (Short Packet)
23	Generic Short WRITE, 2 parameters	SPa (Short Packet)
04	Generic Short READ, no parameters	SPa (Short Packet)
14	Generic Short READ, 1 parameters	SPa (Short Packet)
24	Generic Short READ, 2 parameters	SPa (Short Packet)
05	DCS Write, No Parameter	SPa (Short Packet)
15	DCS Write, 1 Parameter	SPa (Short Packet)
06	DCS Read, No Parameter	SPa (Short Packet)
37	Set Maximum Return Packet Size	SPa (Short Packet)
09	Null Packet, No Data, Note2	LPa (Long Packet)
19	Blanking Packet, no data	LPa (Long Packet)
29	Generic Long Write	LPa (Long Packet)
39	DCS Write Long	LPa (Long Packet)
1E	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)

From the MCU to the Display Module		
2E	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format	LPa (Long Packet)
3E	Packed Pixel Stream, 24-bit RGB, 8-8-8 Format	LPa (Long Packet)
X0 xF	DO NOT USE All unspecified codes are reserved	

Notes:

1. This can be used when the MCU wants to make sure that it is the end of the transmission in High Speed Data Transferring (HSDT) mode.
2. This can be used when data lanes are to be kept in High Speed Data Transferring (HSDT) Mode.

Data Type (DT) from the Display Module (or Other Devices) to the MCU

Table 5-4 Data type from Rx to Tx

From the Display Module to the MCU		
Hex	Description	Short / Long Packet
02h	Acknowledge with Error Report	SPa (Short Packet)
1Ch	DCS Read Long Response	LPa (Long Packet)
21h	DCS Read Short Response, 1 byte returned	SPa (Short Packet)
22h	DCS Read Short Response, 2 byte returned	SPa (Short Packet)
1Ah	Generic Read Long Response	LPa (Long Packet)
11h	Generic Read Short Response, 1 byte returned	SPa (Short Packet)
12h	Generic Read Short Response, 2 byte returned	SPa (Short Packet)

Note: The data type for Generic write/read: 1Ah, 11h, 12 will be disable (ignored packet) if bit DSIG is set to “0”.

The receiver will ignore other Data Type (DT) if they are not defined on tables: “Data Type (DT) from the MCU to the Display Module (or Other Devices)” or “Data Type (DT) from the Display Module (or Other Devices) to the MCU”.

5.3.8 Packet Data (PD) in a Short Packet (SPa)

Packet Data (PD) of the Short Packet (SPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates a Short Packet (SPa) is to be sent. Packet Data (PD) of a Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. The sending order of the Packet Data (PD) is that Data 0 is sent first and the Data 1 is sent last. Bits of Data 1 are set to 0 if the information length is 1 byte. Packet Data (PD) of a Short Packet (SPa), when the length of the information is 1 or 2 bytes and Virtual Channel (VC) is 0, are illustrated for reference purposes below.

Packet Data (PD) information:

- Data 0: 26Hex (Display Command Set (DCS) with 1 Parameter => DI (Data Type (DT)) = 15Hex)
- Data 1: 01Hex (DCS's Parameter)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 26H								8'b 01H								8'b 3EH							
1	0	1	0	1	0	0	0	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-32 Packet Data (PD) for Short Packet (SPa), 2 Bytes Information

Packet Data (PD) information:

- Data 0: 10Hex (DCS without Parameter => DI (Data Type (DT)) = 05Hex)
- Data 1: 00Hex (Null)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-33 Packet Data (PD) for Short Packet (SPa), 1 Byte Information

5.3.9 Word Count (WC) in a Long Packet (LPa)

Word Count (WC) of the Long Packet (LPa) is placed after Data Type (DT) of the Data Identification (DI) and indicates that a Long Packet (LPa) is to be sent. Word Count (WC) indicates the amount of data bytes of the Packet Data (PD) that is to be sent after the Packet Header (PH). The location of the Word Count (WC) in a Long Packet is the same as which of the Packet Data (PD) in a Short Packet (SPa), as shown in Figure 5.4.9-2. Word Count (WC) of the Long Packet (LPa) consists of 2 bytes. The sending order of these 2 bytes of the Word Count (WC) is that the Least Significant (LS) Byte is sent first, and the Most Significant (MS) Byte is sent last. Word Count (WC) of a Long Packet (LPa) is illustrated for reference purposes below.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 29H								8'b 01H								8'b 00H								8'b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-34 Word Count (WC) in a Long Packet (LPa)

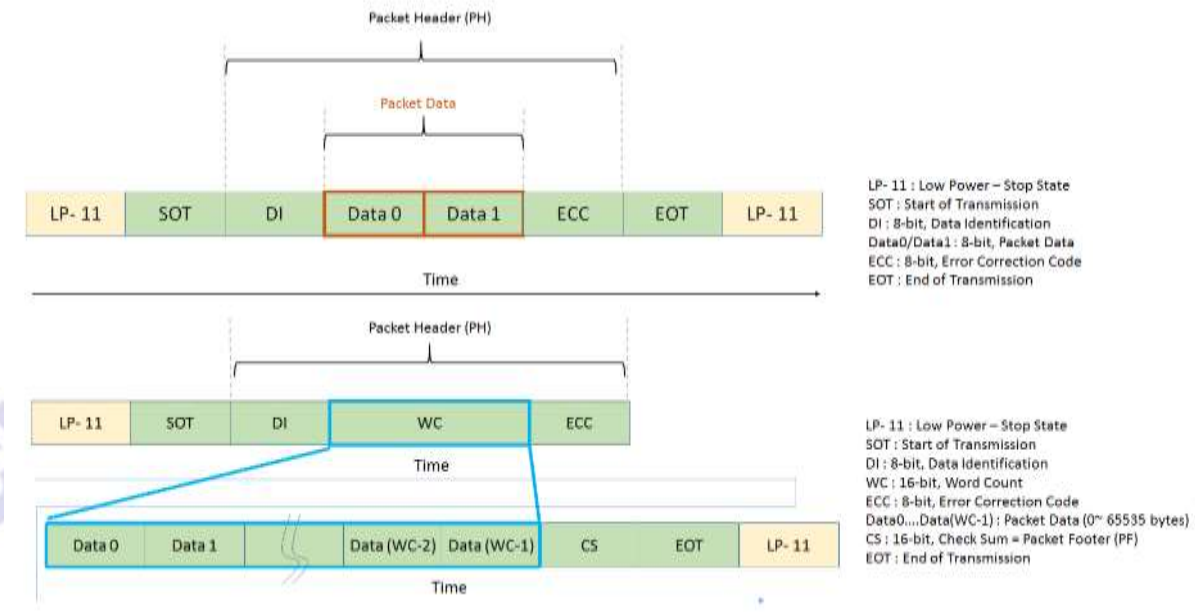


Figure 5-35 Packet Data in Short and Long Packets

5.3.10 Error Correction Code (ECC)

The Error Correction Code (ECC) is a part of Packet Header (PH) and its purpose is to identify an error or errors. The ECC protects the following fields:

- Short Packet (SPa): Data Identification (DI) byte (8 bits: D [0…7]), Packet Data (PD) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7])
- Long Packet (LPa): Data Identification (DI) byte (8 bits: D [0…7]), Word Count (WC) bytes (16 bits: D [8…23]) and ECC (8 bits: P [0…7]) D [23…0] and P [7…0] are illustrated for reference purposes below.

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8’b 05H								8’b 10H								8’b 00H								8’b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-36_D [23:0] and D 7:0] in a Short Packet (SPa)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 29H								8’b 01H								8’b 00H								8’b 06H							
1	0	0	1	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-37 D [23:0] and D 7:0] in a Long Packet (LPa)

Error Correction Code (ECC) can recognize one or several error(s) and can only correct one-bit error. Bits (P [7…0]) of the Error Correction Code (ECC) are defined, where the symbol „^“ presents the XOR function (Pn is 1 if there is odd number of 1, and Pn is 0 if there is even number of 1), as follows.

- P7 = 0
- P6 = 0
- P5 = D10^D11^D12^D13^D14^D15^D16^D17^D18^D19^D21^D22^D23
- P4 = D4^D5^D6^D7^D8^D9^D16^D17^D18^D19^D20^D22^D23
- P3 = D1^D2^D3^D7^D8^D9^D13^D14^D15^D19^D20^D21^D23
- P2 = D0^D2^D3^D5^D6^D9^D11^D12^D15^D18^D20^D21^D22
- P1 = D0^D1^D3^D4^D6^D8^D10^D12^D14^D17^D20^D21^D22^D23
- P0 = D0^D1^D2^D4^D5^D7^D10^D11^D13^D16^D20^D21^D22^D23

P7 and P6 are set to 0 because Error Correction Code (ECC) is based on 64 bit value (D [63…0]), but this implementation is based on 24 bit value (D [23…0]). Therefore, only 6 bits are needed (P [5…0]) for Error Correction Code (ECC).

DI (Data Identification)								Data 0								Data 1								ECC (Error Correction Code)							
8’b 05H								8’b 10H								8’b 00H								8’b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
D0	D1	D2		D4	D5		D7			D10	D11		D13			D16				D20	D21	D22	D23	P0							
D0	D1		D3	D4		D6		D8		D10		D12		D14			D17			D20	D21	D22	D23		P1						
D0		D2	D3		D5	D6			D9		D11	D12			D15			D18		D20	D21	D22				P2					
	D1	D2	D3				D7	D8	D9				D13	D14	D15				D19	D20	D21		D23				P3				
				D4	D5	D6	D7	D8	D9							D16	D17	D18	D19	D20		D22	D23					P4			
										D10	D11	D12	D13	D14	D15	D16	D17	D18	D19		D21	D22	D23						P5		
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-38 XOR Function on Short Packet (SPa)

The sent data bits (D [23…0]) and ECC (P [7…0]) are correctly received if the value of the PO [7…0]) is 00h.

The sent data bits (D [23…0]) and ECC (P [7…0]) are not correctly received if the value of the PO [7…0]) is not 00h.

ECC P [7:0]	1 1 0 0 0 0 0 0	03h
IECC PI [7:0]	1 1 0 0 0 0 0 0	03h
XOR (ECC, IECC) => PO[7:0]	0 0 0 0 0 0 0 0	= 00h => No Error
	LSB … MSB	

Figure 5-39 Internal XOR Calculation between ECC and IECC Values – No Error

ECC P [7:0]	1	1	0	0	0	0	0	0	03h
IECC PI [7:0]	1	1	1	1	0	0	0	0	0Fh
XOR (ECC, IECC) => PO[7:0]	0	0	1	1	0	0	0	0	= 0Ch => Error
	LSB							MSB	

Figure 5-40 Internal XOR Calculation between ECC and IECC Values – Error

The received Error Correction Code (ECC) can be 00h when the Error Correction Code (ECC) function is not used for data values D [23…0] on the transmitter side. The number of the errors (one or more) can be defined when the value of the PO [7…0] is compared to the values in the following table.

Data Bit	PO7	PO6	PO5	PO4	PO3	PO2	PO1	PO0	Hex
D [0]	0	0	0	0	0	1	1	1	07h
D [1]	0	0	0	0	1	0	1	1	0Bh
D [2]	0	0	0	0	1	1	0	1	0Dh
D [3]	0	0	0	0	1	1	1	0	0Eh
D [4]	0	0	0	1	0	0	1	1	13h
D [5]	0	0	0	1	0	1	0	1	15h
D [6]	0	0	0	1	0	1	1	0	16h
D [7]	0	0	0	1	1	0	0	1	19h
D [8]	0	0	0	1	1	0	1	0	1Ah
D [9]	0	0	0	1	1	1	0	0	1Ch
D [10]	0	0	1	0	0	0	1	1	23h
D [11]	0	0	1	0	0	1	0	1	25h
D [12]	0	0	1	0	0	1	1	0	26h
D [13]	0	0	1	0	1	0	0	1	29h
D [14]	0	0	1	0	1	0	1	0	2Ah
D [15]	0	0	1	0	1	1	0	0	2Ch
D [16]	0	0	1	1	0	0	0	1	31h
D [17]	0	0	1	1	0	0	1	0	32h
D [18]	0	0	1	1	0	1	0	0	34h
D [19]	0	0	1	1	1	0	0	0	38h
D [20]	0	0	0	1	1	1	1	1	1Fh
D [21]	0	0	1	0	1	1	1	1	2Fh
D [22]	0	0	1	1	0	1	1	1	37h
D [23]	0	0	1	1	1	0	1	1	3Bh

An error is detected if the value of the PO [7…0] is in Table, and the receiver can correct this one bit error because this found value also defines the location of the corrupt bit, e.g.

- PO [7…0] = 0Eh
- The bit of the data (D [23…0]), that is not correct, is D [3] More than one error is detected if the value of the PO [7…0] is not in Table for example, PO [7…0] = 0Ch.

5.3.11 Packet Data (PD) in a Long Packet (LPa)

Packet Data (PD) of a Long Packet (LPa) is placed after the Packet Header (PH) of a Long Packet (LPa). The amount of the data bytes is defined in the section “Word Count (WC) in a Long Packet (LPa)”.

5.3.12 Packet Footer (PF) in a Long Packet (LPa)

Packet Footer (PF) of a Long Packet (LPa) is placed after the Packet Data (PD) of a Long Packet (LPa). The Packet Footer (PF) is a checksum value that is calculated from the Packet Data of the Long Packet (LPa). The checksum uses a 16-bit Cyclic Redundancy Check (CRC) value which is generated by a polynomial X16+X12+X5+X0, as illustrated below.

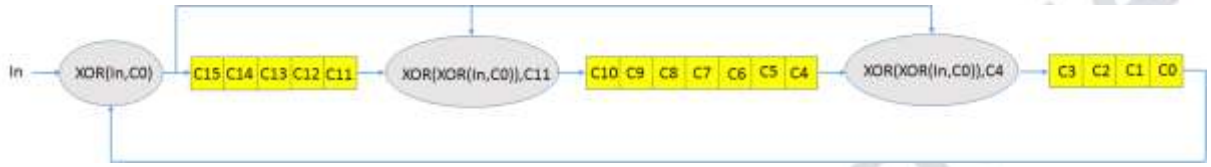
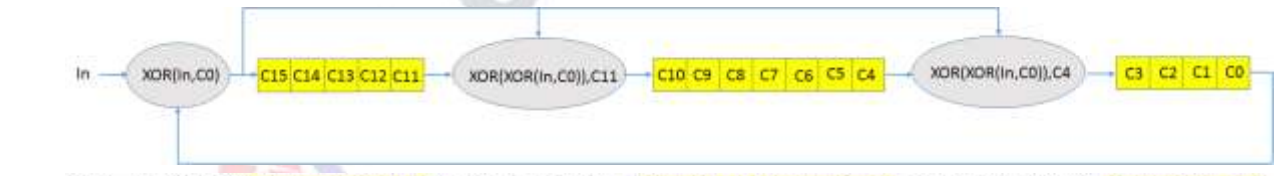


Figure 5-41 16-bit Cyclic Redundancy Check (CRC) Calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit which is inputted into the 16-bit Cyclic Redundancy Check (CRC). An example of the 16-bit Cyclic Redundancy Check (CRC), where the Packet Data (PD) of a Long Packet (LPa) is 01h, is illustrated (step-by-step) below.



Step	In	XOR(In,C0)	C15	C14	C13	C12	C11	XOR(XOR(In,C0),C11 (Step-1))	C10	C9	C8	C7	C6	C5	C4	XOR(XOR(In,C0),C4 (Step-1))	C3	C2	C1	C0	C0
0	X	X	1	1	1	1	1	X	1	1	1	1	1	1	1	X	1	1	1	1	X
1	1(LSB)	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
2	0	1	1	0	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	1	1
3	0	1	1	1	0	1	1	0	0	0	1	1	1	1	1	0	0	0	1	1	1
4	0	1	1	1	1	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1
5	0	1	1	1	1	1	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
6	0	0	0	1	1	1	1	0	0	0	0	0	0	1	1	0	1	0	0	0	0
7	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	0	1	1	0	0	0
8	0(MSB)	0	0	0	0	1	1	1	1	1	0	0	0	0	0	1	1	1	1	0	0
	1byte	CRC result	0	0	0	1	1		1	1	0	0	0	0	0		1	1	1	0	
			MSB																	LSB	

Figure 5-42 CRC Calculation – Packet Data (PD) is 01h

The value of the Packet Footer (PF) is 1E0Eh in this example (Command 01h has been sent), and is illustrated below

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 39H								8’b 01H								8’b 00H								8’b 15H							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (Packet Data)								CRC- LSB								CRC- MSB							
8’b 00H								8’b 0EH								8’b 1EH							
0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-43 Packet Footer (PF) Example

The receiver calculates its checksum value from the received Packet Data (PD). The receiver compares its checksum and the Packet Footer (PF) that the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the checksum of the receiver and Packet Footer (PF) are equal. The received Packet Data (PD) and Packet Footer (PF) are not correct if the checksum of the receiver and Packet Footer (PF) are not equal.

5.4 Packet Transmissions

5.4.1 Display Command Set (DCS)

Display Command Set (DCS), defined in the section “Command 1 Description”, is used from the MCU to the display module. This Display Command Set (DCS) is always defined in the Data 0 of the Packet Data (PD), and is included in Short Packet (SPa) and Long packet (LPa), as illustrated below.

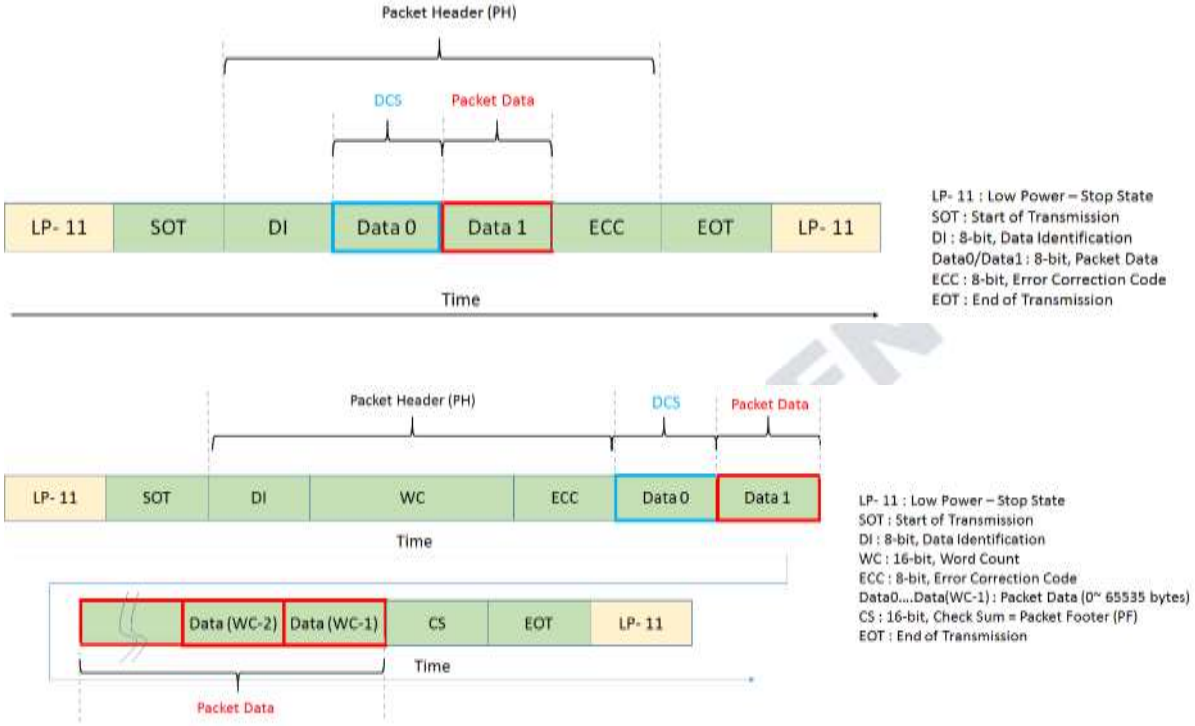


Figure 5-44 Display Command Set (DCS) in Short Packet (SPa) and Long Packet (LPa)

5.4.2 Display Command Set (DCS) Write, No Parameter (DSCWN-S)

"Display Command Set (DCS) Write, No Parameter", which is defined in Data Type (DT, 00 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in a table below.

Command
NOP (00h)
Software Reset (01h)
Sleep In (10h)
Sleep Out (11h)
Normal Display Mode On (13h)
INVOff (20h)
INVOn (21h)
All Pixel Off (22h)
All Pixel On (23h)
Display Off (28h)
Display On (29h)
Tearing Effect Line Off (34h)

A Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0101b
- Packet Data (PD)
  - Data 0: "Sleep In (10h)", Display Command Set (DCS)
  - Data 1: Always 00hex

Error Correction Code (ECC)

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 05H								8'b 10H								8'b 00H								8'b 2CH							
1	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-45 Display Command Set (DCS) Write, No Parameter (DCSWN-S) – Example

5.4.3 Display Command Set (DCS) Write, 1 Parameter (DSCW1-S)

"Display Command Set (DCS) Write, 1 Parameter" (DCSW1-S), which is defined in Data Type (DT, 01 0101b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Command
Gamma Curve Set (26h)
TEON (35h)
MADCTR (36h)
COLMOD (3Ah)
WRDISBV (51h)
WRCTRLD (53h)
WRCABC (55h)
WRCABCMB (5Eh)

Short Packet (SPa) is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 01 0101b
- Packet Data (PD)
  - Data 0: "PMCSET (3Ah)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Error Correction Code (ECC)

This is defined on the Short Packet (SPa) as follows.

DI (Data Identification)								Data 0 (Packet Data)								Data 1 (Packet Data)								ECC (Error Correction Code)							
8'b 15H								8'b 3AH								8'b 01H								8'b 1EH							
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-46 Display Command Set (DCS) Write, 1 Parameter (DCSW1-S) – Example

5.4.4 Display Command Set (DCS) Write, Long (DCSW-L)

"Display Command Set (DCS) Write Long" (DCSW-L), which is defined in Data Type (DT, 11 1001b), is always used in a Long Packet (LPa) from the MCU to the display module. Command (No Parameters) and Write (1 or more parameters) are defined in a table below.

Table 5-5 Display command set write, Long

Command
NOP (00h) Note 1
Software Reset (01h), Note 1
Sleep In (10h) , Note 1
Sleep Out (11h) , Note 1
Normal Display Mode On (13h) , Note 1
INVOff (21h) , Note 1
INVOn (22h) , Note 1
All Pixel Off (22h) , Note 1
All Pixel On (23h) , Note 1
GAMSET (26h) , Note 2
Display Off (28h) , Note 1
Display On (29h) , Note 1
Tearing Effect Line Off (34h) , Note 1
Tearing Effect Line On (35h) , Note 2
MADCTR (36h)
Idle Mode Off (38h) , Note 1
Idle Mode On (39h) , Note 1
COLMOD (3Ah) , Note 2
Tearline (44h)
WRDISBV (51h) , Note 2
WRCTRLD (53h)
WRCABC (55h) , Note 2
WRCABCMB (5Eh)

Notes **:**

1. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, No Parameter.
2. Also Short Packet (SPa) can be used; See Display Command Set (DCS) Write, 1 Parameter.

Long Packet (LPa), when a command (No Parameter) was sent, is defined e.g.

- Data Identification (DI)
  - Virtual Channel (VC, DI[7…6]): 00b
  - Data Type (DT, DI[5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0001h
- Error Correction Code (ECC)
- Packet Data (PD): Data 0: "Sleep In (10h)", Display Command Set (DCS)
- Packet Footer (PF)

This is defined on the Short Packet (SPa) as follows.

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 39H								8'b 01H								8'b 00H								8'b 15H							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (Packet Data)								CRC- LSB								CRC- MSB							
8'b 10H								8'b 06H								8'b 1FH							
0	0	0	0	1	0	0	0	0	1	1	0	0	0	0	0	1	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-47 Display Command Set (DCS) Write, Long (DCSWL-S) with DCS Only– Example

A Long Packet (LPa) with one Write (1 parameter) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0002h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: "Gamma Set (26h)", Display Command Set (DCS)
  - Data 1: 01hex, Parameter of the DCS
- Packet Footer (PF)

DI (Data Identification)								WC - LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 39H								8’b 02H								8’b 00H								8’b 13H							
1	0	0	1	1	1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (DCS)								Data 1 (Parameter)								CRC-LSB								CRC-MSB							
8’b 26H								8’b 01H								8’b D2H								8’b 96H							
0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1	0	1	1	0	1	0	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-48 Display Command Set (DCS) Write, Long with DCS and 1 Parameter – Example

A Long Packet (LPa) with one Write (4 parameters) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 1001b
- Word Count (WC)
  - Word Count (WC): 0005h
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: “Column Address Set (2Ah)” (For example only), Display Command Set (DCS)
  - Data 1: 00hex, 1st Parameter of the DCS, Start Column SC [15…8]
  - Data 2: 12hex, 2nd Parameter of the DCS, Start Column SC [7…0]
  - Data 3: 01hex, 3rd Parameter of the DCS, End Column EC [15…8]
  - Data 4: EFhex, 4th Parameter of the DCS, End Column EC [7…0]
- Packet Footer (PF)

DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8’b 39H								8’b 05H								8’b 00H								8’b 36H							
1	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0 (DCS)								Data 1 (1st Parameter)								Data 2 (2nd Parameter)								Data 3 (3rd Parameter)							
8’b 2AH								8’b 00H								8’b 12H								8’b 01H							
0	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4 (4th Parameter)								CRC – LSB								CRC – MSB							
8’b EFH								8’b BDH								8’b 2AH							
1	1	1	1	0	1	1	1	1	0	1	1	1	1	0	1	0	1	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-49 Display Command Set (DCS) Write, Long with DCS and 4 Parameter – Example

5.4.5 Display Command Set (DCS) Read, No Parameter (DCSRN-S)

"Display Command Set (DCS) Read, No Parameter" (DCSRN-S), which is defined in Data Type (DT, 00 0110b), is always used in a Short Packet (SPa) from the MCU to the display module. These commands are defined in the table below.

Table 5-6 Display Command Set (DCS) Read

Command
RDDID (04h)
RDDPM (0Ah)
RDDMADCTR (0Bh)
RDDCOLMOD (0Ch)
RDDIM (0Dh)
RDDSM (0Eh)
RDDSDR (0Fh)
GSL (45h)
RDDISBV (52h)
RDCTRLD (54h)
RDCABC (56h)
RDCABCMB (5Fh)
RDID1 (DAh)
RDID2 (DBh)
RDID3 (DCh)

The MCU has to define to the display module the maximum size of the returned packet. The command, which is used for this purpose, is "Set Maximum Return Packet Size" (SMRPS-S), which Data Type (DT) is 11 0111b and is used in a Short Packet (SPa) before the MCU can send "Display Command Set (DCS) Read, No Parameter" to the display module. This sequence is illustrated for reference purposes below.

➢ Step1

The MCU sends "Set Maximum Return Packet Size" (Short Packet (SPa)) (SMRPS-S) to the display module when it wants to return one byte from the display module.

➢ Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 11 0111b

➢ Maximum Return Packet Size (MRPS)
  - Data 0: 01hex
  - Data 1: 00hex

➢ Error Correction Code (ECC)

DI (Data Identification)								MRPS – LSB								MRPS – MSB								ECC (Error Correction Code)							
8’b 37H								8’b 01H								8’b 00H								8’b 1DH							
1	1	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-50 Set Maximum Return Packet Size (SMRPS-S) – Example

➢ Step 2

The MCU wants to receive the value of the “Read ID1 (DAh)” from the display module when the MCU sends “Display Command Set (DCS) Read, No Parameter” to the display module.

➢ Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 00 0110b

➢ Packet Data (PD)
- Data 0: “Read ID1 (DAh)”, Display Command Set (DCS)
- Data 1: Always 00hex

➢ Error Correction Code (ECC)

DI (Data Identification)								Data 0 (DCS)								Data 1 (Always 8’b 00H)								ECC (Error Correction Code)							
8’b 06H								8’b DAH								8’b 00H								8’b 1FH							
0	1	1	0	0	0	0	0	0	1	0	1	1	0	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-51 Display Command Set (DCS) Read, No Parameter (DCSRN – S) – Example

➢ Step 3

The display module can send 2 different information to the MCU after Bus Turnaround (BTA):

1. An acknowledge with Error Report (AwER), which is used in a Short Packet (SPa), if there is an error when receiving a command. See the section “Acknowledge with Error Report (AwER)”.
2. Information of the received command, which can be a Short Packet (SPa) or a Long Packet (LPa).

5.4.6 Null Packet, No Data (NP-L)

"Null Packet, No Data" (NP-L), which is defined in Data Type (DT, 001001b), is always used in a Long Packet (LPa) from the MCU to the display module. The purpose of this command is to keep data lanes in the high speed mode (HSDT) if necessary. The display module can ignore the Packet Data (PD) that the MCU sends.

A Long Packet (LPa) with 5 random data bytes of the Packet Data (PD) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1001b
- Word Count (WC)
  - Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
  - Data 0: 89hex (Random data)
  - Data 1: 23hex (Random data)
  - Data 2: 12hex (Random data)
  - Data 3: A2hex (Random data)
  - Data 4: E2hex (Random data)
- Packet Footer (PF)

DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 09H								8'b 05H								8'b 00H								8'b 30H							
1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0								Data 1								Data 2								Data 3							
8'b 89H								8'b 23H								8'b 12H								8'b A2H							
1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4								CRC – LSB								CRC – MSB							
8'b E2H								8'b 59H								8'b 29H							
0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-52 Null Packet, No Data (NP- L) – Example

5.4.7 End of Transmission Packet (EoTP)

"End of Transmission Packet" (EoTP), which is an interface level function and defined in Data Type (DT, 00 1000b), is always used in a Short Packet (SPa) from the MCU to the display module. The purpose of this command is to terminate the high Speed Data Transmission (HSDT) mode properly when EoTP is added after the last payload packet before "End of Transmission" (EoT).The MCU can decide if it wants to use the "End of Transmission Packet" (EoTP) or not. The display shall have the capability to support both. That is, if the MCU applies the EoTP, it shall report the "DSI Protocol Violation Error" when the EoTP is not detected in the High-Speed (HS). The display module error reporting shall be enabled/disabled statistically, according to the module application. The display module does or does not receive "End of Transmission Packet" (EoTP) from the MCU during the Low Power Data Transmission (LPDT) mode before "Mark-1" (= leaving the Escape mode) which ends the Low Power Data Transmission (LPDT) mode. The display module is not allowed to send "End of Transmission Packet" (EoTP) to the MCU during the Low Power Data Transmission (LPDT) mode. The summary of the receiving and transmitting EoTP is listed below.

Direction	Display Module (DM) in High Speed Data Transmission (HSDT)	Display Module (DM) in Low Power Data Transmission (LPDT)
MCU=> Display Module	Support with and without EoTP	Support with and without EoTP
Display Module => MCU	HS mode is not available (EoTP is not available)	EoTP cannot be sent by the Display Module (DM)

A Short Packet (SPa) using a fixed format is as follows:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 1000b
- Packet Data (PD)
  - Data 0: 0Fhex
  - Data 1: 0Fhex
- Error Correction Code

DI (Data Identification)								Data 0								Data 1								ECC (Error Correction Code)							
8'b 08H								8'b 0FH								8'b 0FH								8'b 01H							
0	0	0	1	0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-53 End of Transmission Packet (EoTP)

Some examples of the "End of Transmission Packet" (EoTP) are illustrated for reference purposes below.

Figure 5-54 End of Transmission Packet (EoTP) – Example

5.4.8 Acknowledge with Error Report (AwER)

"Acknowledge with Error Report" (AwER), which is defined in Data Type (DT, 00 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. The Packet Data (PD) can include bits, which define the current error, when the corresponding bit is set to 1, as defined in the following table.

Table 5-7 Acknowledge with Error Report

Bit	Description
0	SoT Error
1	SoT Sync Error
2	EoT Sync Error
3	Escape Mode Entry Command Error
4	Low-Power Transmit Sync Error
5	Any Protocol Timer Time-Out
6	False Control Error
7	Contention is Detected on the Display Module
8	ECC Error, single-bit (detected and corrected)
9	ECC Error, multi-bit (detected, not corrected)
10	Checksum Error (Long Packet only)
11	DSI Data Type (DT) Not Recognized
12	DSI Virtual Channel (VC) ID Invalid
13	Invalid Transmission Length
14	Reserved, Set to 0 internally
15	DSI Protocol Violation

These errors are included in all packages that have been received from the MCU to the display module before the Bus Turnaround (BTA). The display module ignores the received packet which includes error or errors.

Acknowledge with Error Report (AwER) of a Short Packet (SPa) is defined as:

- Data Identification (DI)
  - Virtual Channel (VC, DI [7…6]): 00b
  - Data Type (DT, DI [5…0]): 00 0010b
- Packet Data (PD)
  - Bit 8: ECC Error, single-bit (detected and corrected)
  - AwER: 0100h
- Error Correction Code (ECC)

DI (Data Identification)								AwER – LSB								AwER – MSB								ECC (Error Correction Code)							
8'b 02H								8'b 00H								8'b 01H								8'b 3AH							
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0	1	1	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-55 Acknowledge with Error Report (AwER) – Example

It is possible that the display module receives several packets, which include errors, from the MCU before the MCU performs the Bus Turnaround (BTA). Some examples are illustrated for reference purposes below.

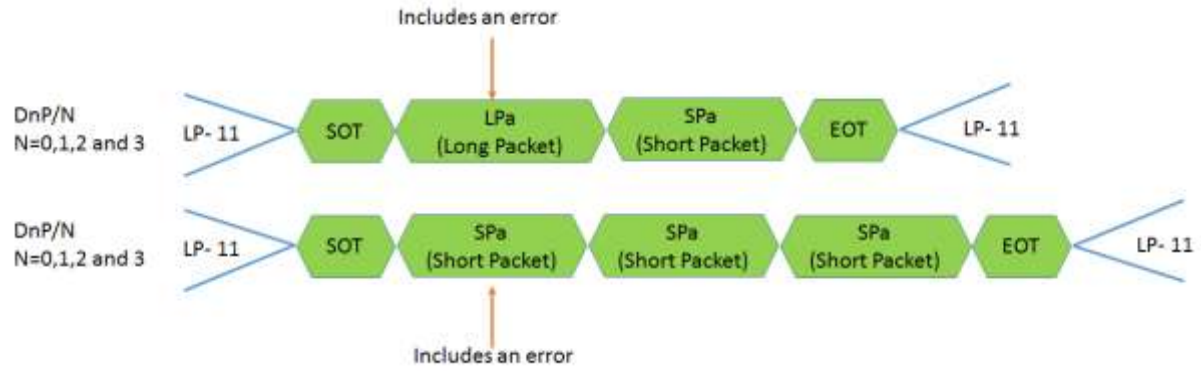


Figure 5-56 Error Packets

Therefore, a method is needed to check if there are errors in the previous packets. These errors of the previous packets can be detected by "Read Display Signal Mode (0Eh)" and "Read Number of the Errors on DSI (05h)" commands. The bit D0 of the "Read Display Signal Mode (0Eh)" command will be set to 1 if a received packet includes an error. The amount of packets, which include an ***ECC*** *or* ***CRC*** error, is calculated in the RDNUMED register, which can read "Read Number of the Errors on DSI (05h)" command. This command also sets the RDNUMED register to 00h and set the bit D0 of the "Read Display Signal Mode (0Eh)" command to 0 after the MCU has read the RDNUMED register from the display module. The functionality of the RDNUMED register is illustrated for reference purposes below.

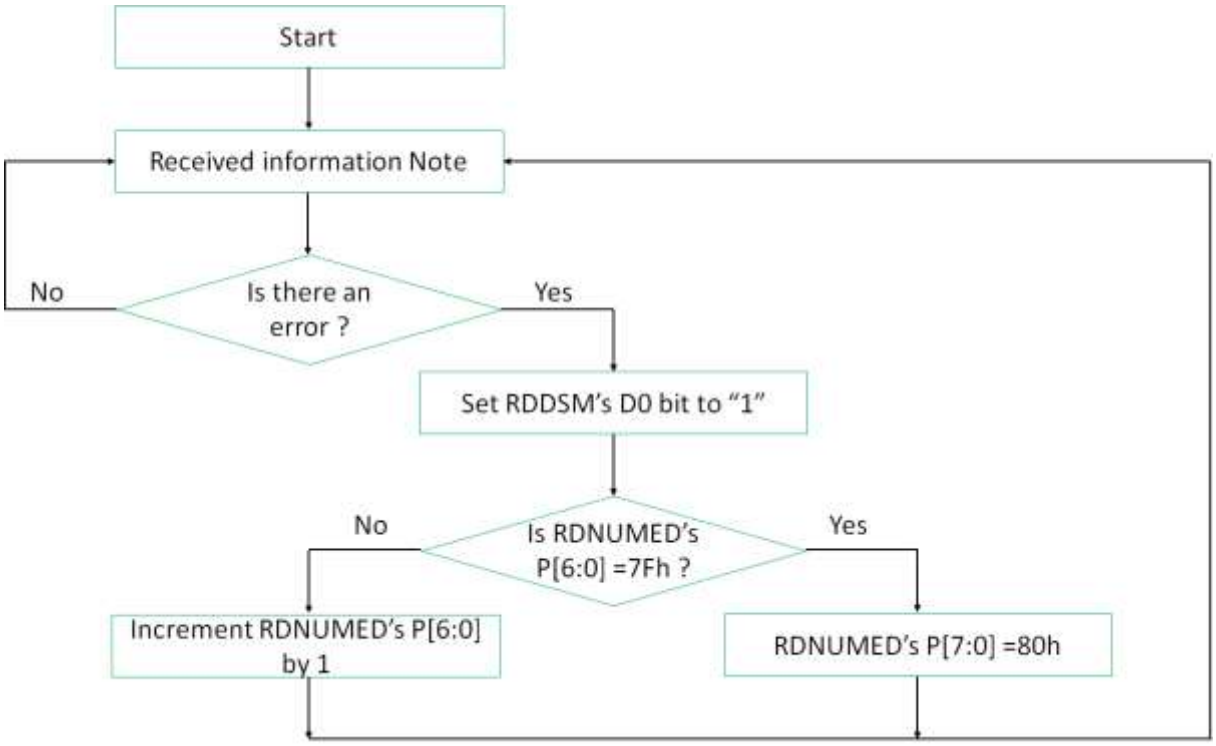


Figure 5-57 Flow Chart for Errors on DSI

Notes:

1. This information can be Interface or Packet Level Communication, but it is always from the MCU to the display module.
2. CRC or ECC error

5.4.9 DCS Read Long Response (DCSRR-L)

"DCS Read Long Response" (DCSRR-L), which is defined in Data Type (DT, 011100b), is always used in a Long Packet (LPa) from the display module to the MCU. "DCS Read Long Response" (DCSRR-L) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Long Packet (LPa), which includes 5 data bytes of the Packet Data (PD), defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 01 1100b
- Word Count (WC)
- Word Count (WC): 0005hex
- Error Correction Code (ECC)
- Packet Data (PD):
- Data 0: 89hex
- Data 1: 23hex
- Data 2: 12hex
- Data 3: A2hex
- Data 4: E2hex
- Packet Footer (PF)

DI (Data Identification)								WC – LSB (Word Count – LSB)								WC – MSB (Word Count – MSB)								ECC (Error Correction Code)							
8'b 1CH								8'b 05H								8'b 00H								8'b 29H							
0	0	1	1	1	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 0								Data1								Data2								Data3							
8'b 89H								8'b 23H								8'b 12H								8'b A2H							
1	0	0	1	0	0	0	1	1	1	0	0	0	1	0	0	0	1	0	0	1	0	0	0	0	1	0	0	0	1	0	1
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Data 4								CRC – LSB								CRC – MSB							
8'b E2H								8'b 59H								8'b 29H							
0	1	0	0	0	1	1	1	1	0	0	1	1	0	1	0	1	0	0	1	0	1	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-58 DCS Read Long Response (DCSRR-L) – Example

5.4.10 DCS Read Short Response, 1 Byte Returned (DCSRR1-S)

"DCS Read Short Response, 1 Byte Returned" (DCSRR1-S), which is defined in Data Type (DT, 10 0001b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 1 Byte Returned (DCSRR1-S) is used when the display module wants to respond to a DCS Read command, which the
MCU has sent to the display module.
A Short Packet (SPa) is defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 10 0001b
- Packet Data (PD)
- Data 0: 45hex
- Data 1: 00hex (Always)
- Error Correction Code (ECC)

DI (Data Identification)								Data0 (Packet Data)								Data1 (Always 8'b 00h)								ECC (Error Correction Code)							
8'b 21H								8'b 45H								8'b 00H								8'b 01H							
1	0	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-59 DCS Read Short Response, 1Byte Return (DCSRR1-S) – Example

5.4.11 DCS Read Short Response, 2 Byte Returned (DCSRR2-S)

"DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S), which is defined in Data Type (DT, 10 0010b), is always used in a Short Packet (SPa) from the display module to the MCU. "DCS Read Short Response, 2 Bytes Returned" (DCSRR2-S) is used when the display module wants to respond to a DCS Read command, which the MCU has sent to the display module.

A Short Packet (SPa) is defined as:

- Data Identification (DI)
- Virtual Channel (VC, DI [7…6]): 00b
- Data Type (DT, DI [5…0]): 10 0010b
- Packet Data (PD)
- Data 0: 45hex
- Data 1: 32hex
- Error Correction Code (ECC)

DI (Data Identification)								Data 0 (Packet Data)								Data1								ECC (Error Correction Code)							
8'b 22H								8'b 45H								8'b 32H								8'b 0FH							
0	1	0	0	0	1	0	0	1	0	1	0	0	0	1	0	0	1	0	0	1	1	0	0	1	1	1	1	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7	B0	B1	B2	B3	B4	B5	B6	B7
LSB							MSB	LSB							MSB	LSB							MSB	LSB							MSB

Time

Figure 5-60 DCS Read Short Response, 2Byte Returned (DCSRR2-S) – Example

5.5 Communication Sequences

5.5.1 General

The communication sequences can be done on interface or packet levels between the MCU and the display module. See sections “Interface Level Communication” and “Packet Level Communication”. This communication sequence description is for DSI data lanes (D3P/N, D2P/N, D1P/N and D0P/N), and it is assumed that the needed low level communication is done on DSI Clock lane (CLKP/N) automatically. See the section “DSI CLK Lanes”. Functions of the interface level communication are described in the following table.

Table 5-8 Interface Level Communication

Interface Mode	Abbreviation	Interface Action Description
Low Power	LP-11	Stop state
	LPDT	Low power data transmission
	ULPS	Ultra- Low power state
	RAR	Remote application reset
	TEE	Tearing effect event (Not supported)
	ACK	Acknowledge (No error)
	BTA	Bus turnaround
High Speed	HSDT	High speed data transmission

Functions of the packet level communication are described on the following table.

Table 5-9 Packet level communication

Packet Sender	Abbreviation	Packet Size	Packet Description
MCU	DCSW1-S	SPa	DCS Write, 1 Parameter
	DCSWN-S	SPa	DCS Write, No Parameter
	DCSW-L	LPa	DCS Write, Long
	DCSRN-S	SPa	DCS Read, No Parameter
	SMRPS-S	SPa	Set maximum return packet size
	NP-L	LPa	Null packet, No data
Display Module	AwER	SPa	Acknowledge with error report
	DCSRR-L	LPa	DCS Read, Long Response
	DCSRR1-S	SPa	DCS Read, Short Response
	DCSRR2-S	SPa	DCS Read, Short Response

5.5.2 Sequences –DCS Write, 1 Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” is defined on chapter “Display Command Set (DCS) Write, 1 Parameter (DCSW1-S)” and example sequences, how this packet is used is described on following tables.

Table 5-10 DCS Write,1 parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 5-11 DCS Write,1 parameter Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

Table 5-12 DCS Write,1 parameter Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW1-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4		LP-11	=>			
5		BTA	<=>	BTA		Interface control change from the MCU to the display module
6		-	<=	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	<=	ACK		No error
9		-	<=	LP-11		
10		BTA	<=>	BTA		Interface control change from the display module to the MCU
11		LP-11	=>	-		End
12						
13		-	<=	LPDT	AwER	Error report
14		-	<=	LP-11		
15		BTA	<=>	BTA		
16	-	LP-11	=>	-	-	End

5.5.3 Sequences –DCS Write, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” is defined on chapter “Display Command Set (DCS) Write, No Parameter (DCSWN-S)” and example sequences, how this packet is used, is described on following tables.

Table 5-13 DCS Write, No parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 5-14 DCS Write, No parameter Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

Table 5-15 DCS Write, No parameter Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSWN-S	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4		LP-11	=>			
5		BTA	<=>	BTA		Interface control change from the MCU to the display module
6		-	<=	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	<=	ACK		No error
9		-	<=	LP-11		
10		BTA	<=>	BTA		Interface control change from the display module to the MCU
11		LP-11	=>	-		End
12						
13		-	<=	LPDT	AwER	Error report
14		-	<=	LP-11		
15		BTA	<=>	BTA		
16	-	LP-11	=>	-	-	End

5.5.4 Sequences –DCS Write, Long Sequence

A Long Packet (LPa) of “Display Command Set (DCS) Write Long (DCSW-L)” is defined on chapter “Display Command Set (DCS) Write Long (DCSW-L)” and example sequences, how this packet is used, is described on following tables.

Table 5-16 DCS Write, Long Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	LPDT	=>	-	-	
3	-	LP-11	=>	-	-	End

Table 5-17 DCS Write, Long Sequence – Example 2

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4	-	LP-11	=>	-	-	End

Table 5-18 DCS Write, Long Sequence – Example 3

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	DCSW-L	HSDT	=>	-	-	
3	EoTP	HSDT	=>	-	-	End of Transmission Packet
4		LP-11	=>			
5		BTA	<=>	BTA		Interface control change from the MCU to the display module
6		-	<=	LP-11		If no error => goto line 8 If error => goto line 13
7						
8		-	<=	ACK		No error
9		-	<=	LP-11		
10		BTA	<=>	BTA		Interface control change from the display module to the MCU
11		LP-11	=>	-		End
12						
13		-	<=	LPDT	AwER	Error report
14		-	<=	LP-11		
15		BTA	<=>	BTA		
16	-	LP-11	=>	-	-	End

5.5.5 Sequences –DCS Read, No Parameter Sequence

A Short Packet (SPa) of “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” is defined on chapter “Display Command Set (DCS) Read, No Parameter (DCSRN-S)” and example sequences, how this packet is used, is described on following tables.

Table 5-19 DCS Read, No Parameter Sequence – Example 1

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	SMRPS-S	HSDT	=>	-	-	Define how many data byte is wanted to read: 1 byte
3	DCSRN-S	HSDT	=>	-	-	wanted to get a response ID1 (DAh)
4	EoTP	HSDT	=>	-	-	End of Transmission Packet
5	-	LP-11	=>	-	-	
6	-	BTA	<=>	BTA	-	Interface control change from the MCU to the display module
7	-	-	<=	LP-11	-	If no error => goto line 9 If error => goto line 14 If error is corrected by ECC => go to line 19
8						
9	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
10	-	-	<=	LP-11	-	
11	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
12	-	LP-11	=>	-	-	End
13						
14	-	-	<=	LPDT	AwER	Error report
15	-	-	<=	LP-11	-	
16	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
17	-	LP-11	=>	-	-	End
18						
19	-	-	<=	LPDT	DCSRR1-S	Responded 1 byte return
20	-	-	<=	LPDT	AwER	Error Report (Error is Corrected by ECC)
21	-	-	<=	LP-11	-	
22	-	BTA	<=>	BTA	-	Interface control change from the display module to the MCU
23	-	LP-11	=>		-	End

5.5.6 Sequences –Null Packet, No Data Sequence

A Long Packet (LPa) of “Null Packet, No Data (NP-L)” is defined on chapter “Null Packet, No Data (NP-L)” and example sequences, how this packet is used, is described on following tables.

Table 5-20 Null Packet, No Data Sequence – Example

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>			End of transmission Packet
4	-	LP-11	=>	-	-	End

5.5.7 Sequences –End of Transmission Packet

A Short Packet (SPa) of “End of Transmission (EoT)” is defined on chapter “End of Transmission Packet (EoT)” and an example sequences, how this packet is used, is described on following tables.

Table 5-21 End of Transmission Packet – Example

Line	MCU		Interface Direction	Display Module		Comment
	Packet Sender	Interface Mode Control		Interface Mode Control	Packet Sender	
1	-	LP-11	=>	-	-	Start
2	NP-L	HSDT	=>	-	-	Only high speed data transmission is used.
3	EoTP	HSDT	=>			End of transmission Packet
4	-	LP-11	=>	-	-	End

5.6 Video Mode Communication

Video Mode peripherals require pixel data delivered in real time. This section specifies the format and timing of DSI traffic for this type of display module.

5.6.1 Transmission Packet Sequences

DSI supports several formats, or packet sequences, for Video Mode data transmission. The peripheral's timing requirements dictate which format is appropriate. In the following sections, *Burst Mode* refers to time-compression of the RGB pixel (active video) portion of the transmission. In addition, these terms are used throughout the following sections:

- Non-Burst Mode with Sync Pulses – enables the peripheral to accurately reconstruct original video timing, including sync pulse widths.
- Non-Burst Mode with Sync Events – similar to above, but accurate reconstruction of sync pulse widths is not required, so a single Sync Event is substituted.
- Burst mode – RGB pixel packets are time-compressed, leaving more time during a scan line for LP mode (saving power) or for multiplexing other transmissions onto the DSI link.

In the following figures the Blanking or Low-Power Interval (BLLP) is defined as a period during which video packets such as pixel-stream and sync event packets are not actively transmitted to the peripheral. To enable PHY synchronization the host processor should periodically end HS transmission and drive the Data Lanes to the LP state. This transition should take place at least once per frame; shown as LPM in the figures in this section. It is recommended to return to LP state once per scan-line during the horizontal blanking time. Regardless of the frequency of BLLP periods, the host processor is responsible for meeting all documented peripheral timing requirements. Note, at lower frequencies BLLP periods will approach, or become, zero, and burst mode will be indistinguishable from non-burst mode.

During the BLLP the DSI Link may do any of the following:

- Remain in Idle Mode with the host processor in LP-11 state and the peripheral in LP-RX
- Transmit one or more non-video packets from the host processor to the peripheral using Escape Mode
- Transmit one or more non-video packets from the host processor to the peripheral using HS Mode
- If the previous processor-to-peripheral transmission ended with BTA, transmit one or more packets from the peripheral to the host processor using Escape Mode
- Transmit one or more packets from the host processor to a different peripheral using a different Virtual Channel ID

The sequence of packets within the BLLP or RGB portion of a HS transmission is arbitrary. The host processor may compose any sequence of packets, including iterations, within the limits of the packet format definitions. For all timing cases, the first line of a frame shall start with VS; all other lines shall start with HS. This is also true in the special case when VSA+VBP=0. Note that the position of synchronization packets, such as VS and HS, in time is of utmost importance since this has a direct impact on the visual performance of the display panel.

Normally, RGB pixel data is sent with one full scan line of pixels in a single packet. If necessary,

a horizontal scan-line of active pixels may be divided into two or more packets. However, individual pixels shall not be split across packets.

Transmission packet components used in the figures in this section are defined in figure below unless otherwise specified.

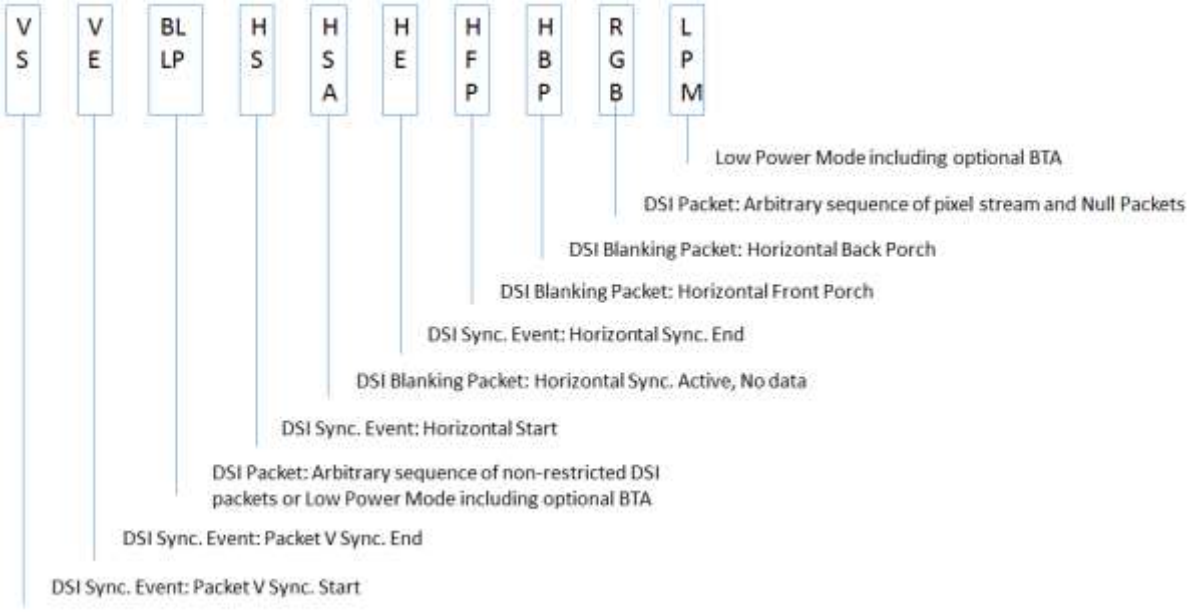


Figure 5-61 DSI Video Mode Interface Timing Legend

If a peripheral timing specification for HBP or HFP minimum period is zero, the corresponding Blanking Packet may be omitted. If the HBP or HFP maximum period is zero, the corresponding blanking packet shall be omitted.

5.6.2 Non-Burst Mode with Sync Pulses

With this format, the goal is to accurately convey DPI-type timing over the DSI serial Link. This includes matching DPI pixel-transmission rates, and widths of timing events like sync pulses. Accordingly, synchronization periods are defined using packets transmitting both start and end of sync pulses. An example of this mode is shown in figure below.

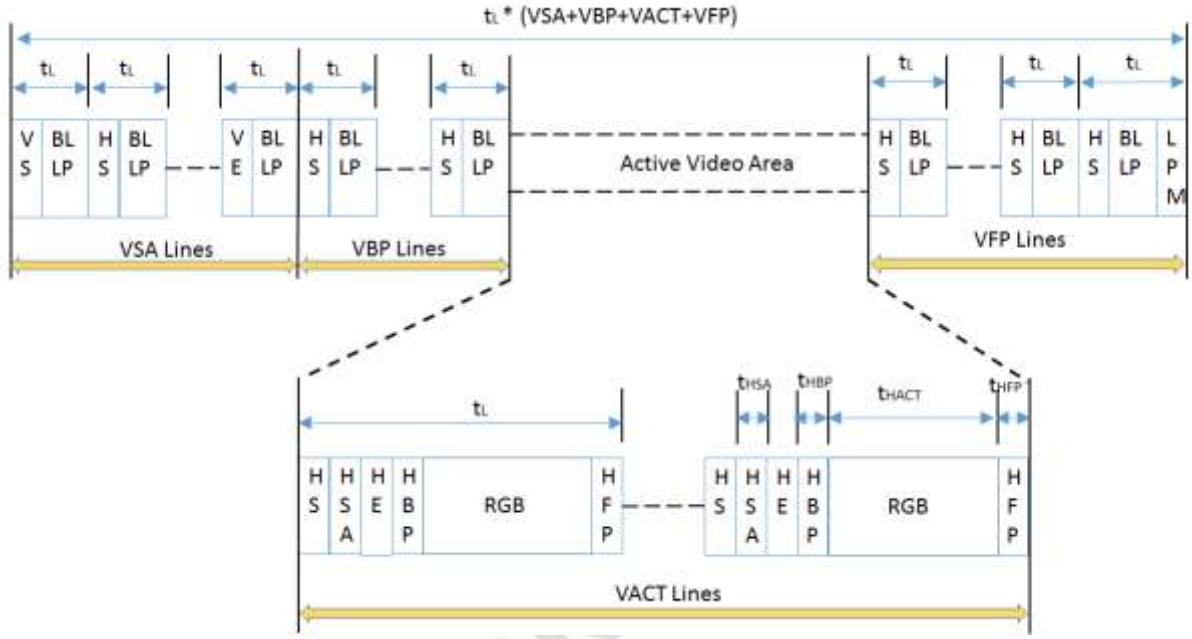


Figure 5-62 DSI Video Mode Interface Timing: Non-Burst Transmission with Sync Start and End

Normally, periods shown as HSA (Horizontal Sync Active), HBP (Horizontal Back Porch) and HFP (Horizontal Front Porch) are filled by Blanking Packets, with lengths (including packet overhead) calculated to match the period specified by the peripheral's data sheet. Alternatively, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.6.3 Burst Mode

In this mode, blocks of pixel data can be transferred in a shorter time using a time-compressed burst format. This is a good strategy to reduce overall DSI power consumption, as well as enabling larger blocks of time for other data transmissions over the Link in either direction. There may be a line buffer or similar memory on the peripheral to accommodate incoming data at high speed. Following HS pixel data transmission, the bus goes to Low Power Mode, during which it may remain idle, i.e. the host processor remains in LP-11 state, or LP transmission may take place in either direction. If the peripheral takes control of the bus for sending data to the host processor, its transmission time shall be limited to ensure data underflow does not occur from its internal buffer memory to the display device. An example of this mode is shown in figure below.

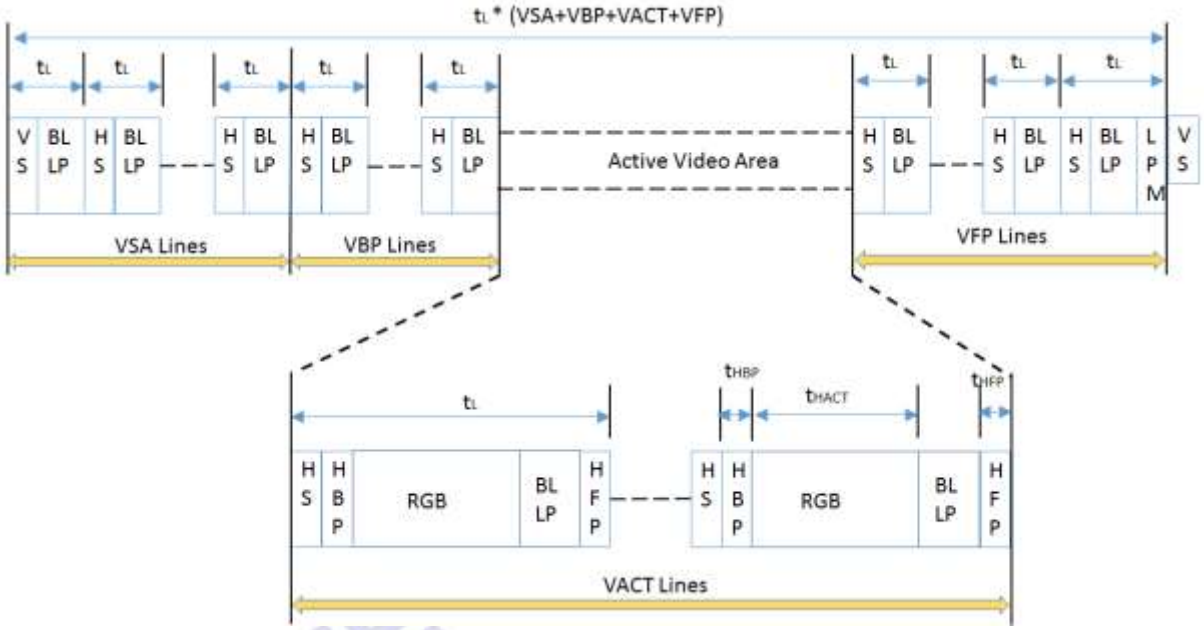


Figure 5-63 DSI Video Mode Interface Timing: Burst Transmission

Similar to the Non-Burst Mode scenario, if there is sufficient time to transition from HS to LP mode and back again, a timed interval in LP mode may substitute for a Blanking Packet, thus saving power.

5.7 Display Data Format

5.7.1 16-bit per Pixel, Long Packet, Data Type 001110 (0Eh)

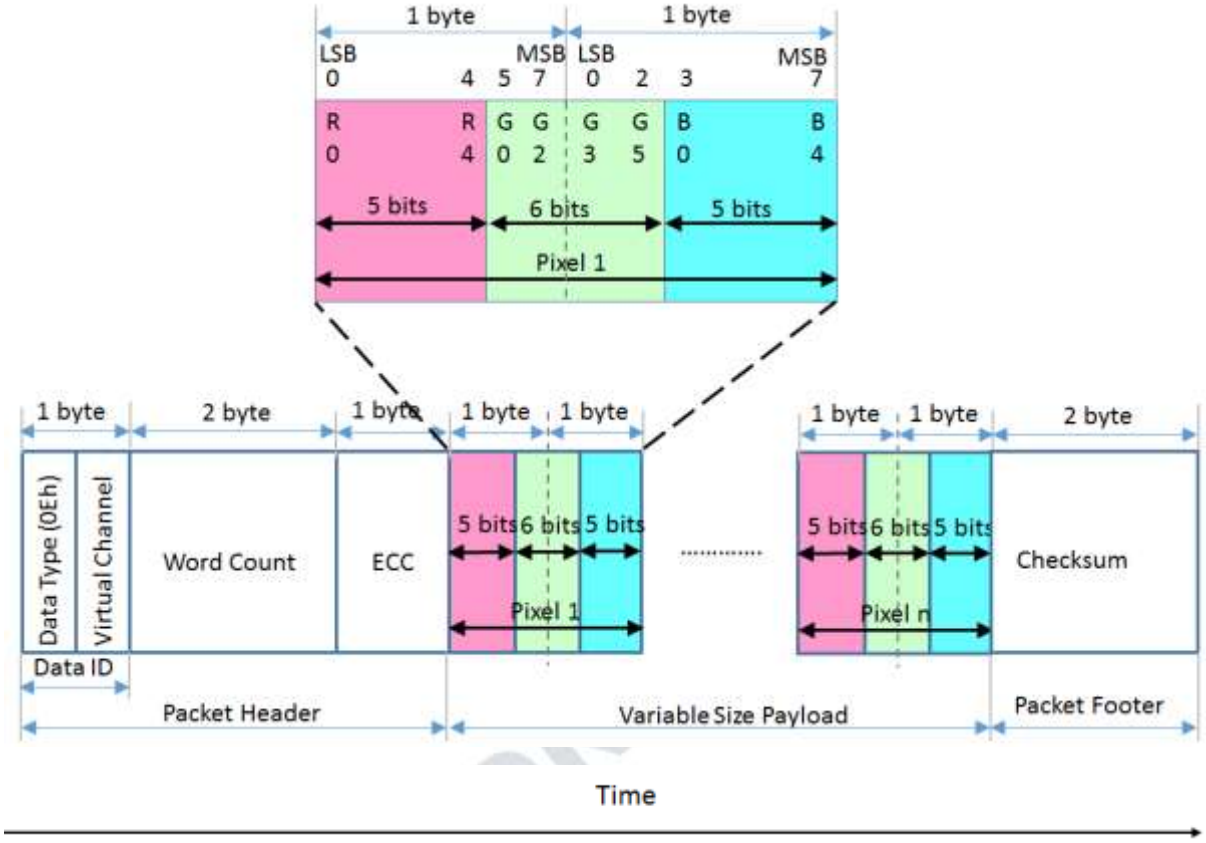


Figure 5-64 16-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 16-Bit Format is a Long packet used to transmit image data formatted as 16-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte checksum. Pixel format is five bits red, six bits green, five bits blue, in that order. Note that the “Green” component is split across two bytes. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every two bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of two bytes.
Normally, the display module has no frame buffer of its own, so all image data shall be supplied by the host processor at a sufficiently high rate to avoid flicker or other visible artifacts.

5.7.2 18-bit per Pixel, Long Packet, Data Type 011110 (1Eh)

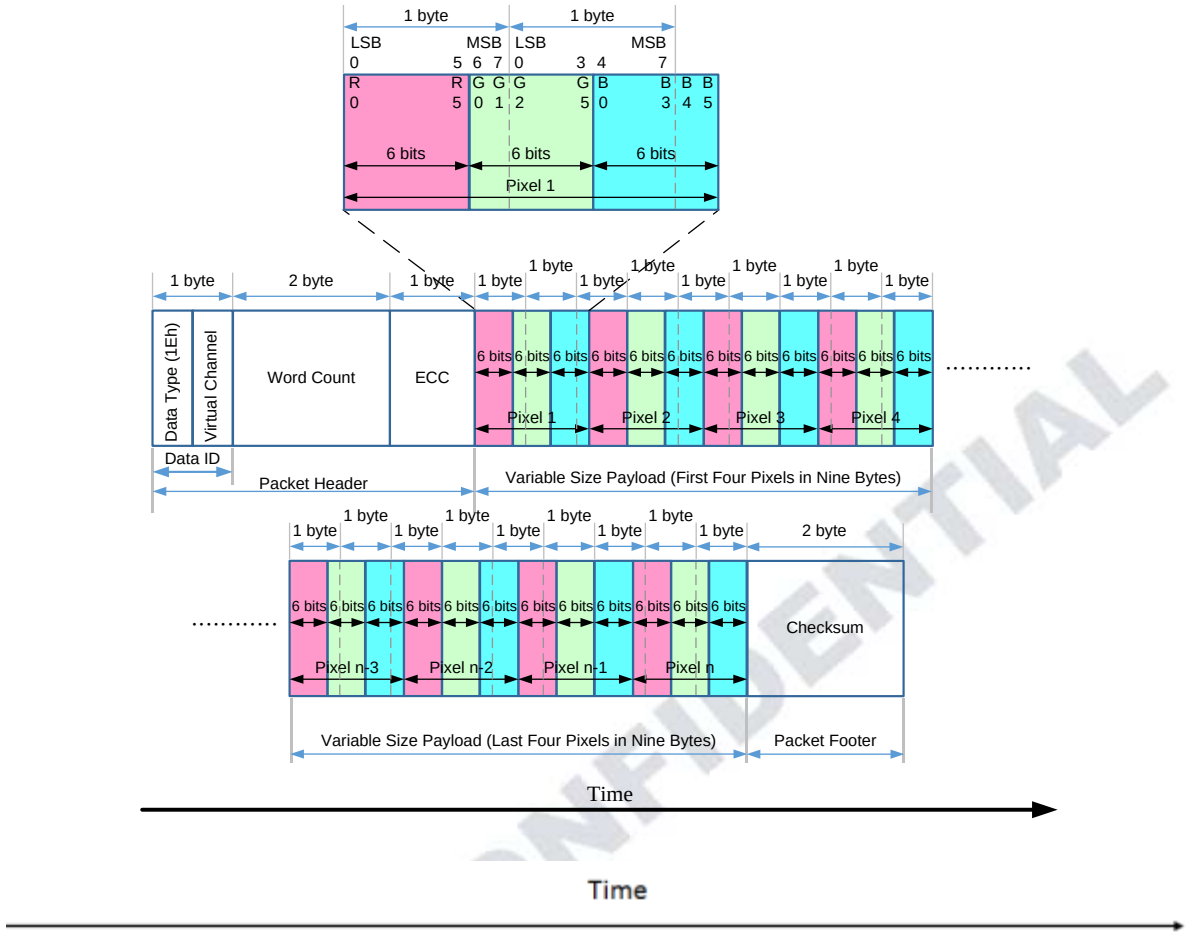


Figure 5-65 18-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 18-Bit Format (Packed) is a Long packet. It is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. Pixel format is red (6 bits), green (6 bits) and blue (6 bits), in that order. Within a color component, the LSB is sent first, the MSB last. Note that pixel boundaries only align with byte boundaries every four pixels (nine bytes). Preferably, display modules employing this format have a horizontal extent (width in pixels) evenly divisible by four, so no partial bytes remain at the end of the display line data. If the active (displayed) horizontal width is not a multiple of four pixels, the transmitter shall send additional fill pixels at the end of the display line to make the transmitted width a multiple of four pixels. The receiving peripheral shall not display the fill pixels when refreshing the display device.

For example, if a display device has an active display width of 399 pixels, the transmitter should send 400 pixels in one or more packets. The receiver should display the first 399 pixels and discard the last pixel of the transmission.

With this format, the total line width (displayed plus non-displayed pixels) should be a multiple of four pixels (nine bytes).

5.7.3 18-bit per Pixel, Long Packet, Data Type 101110 (2Eh)

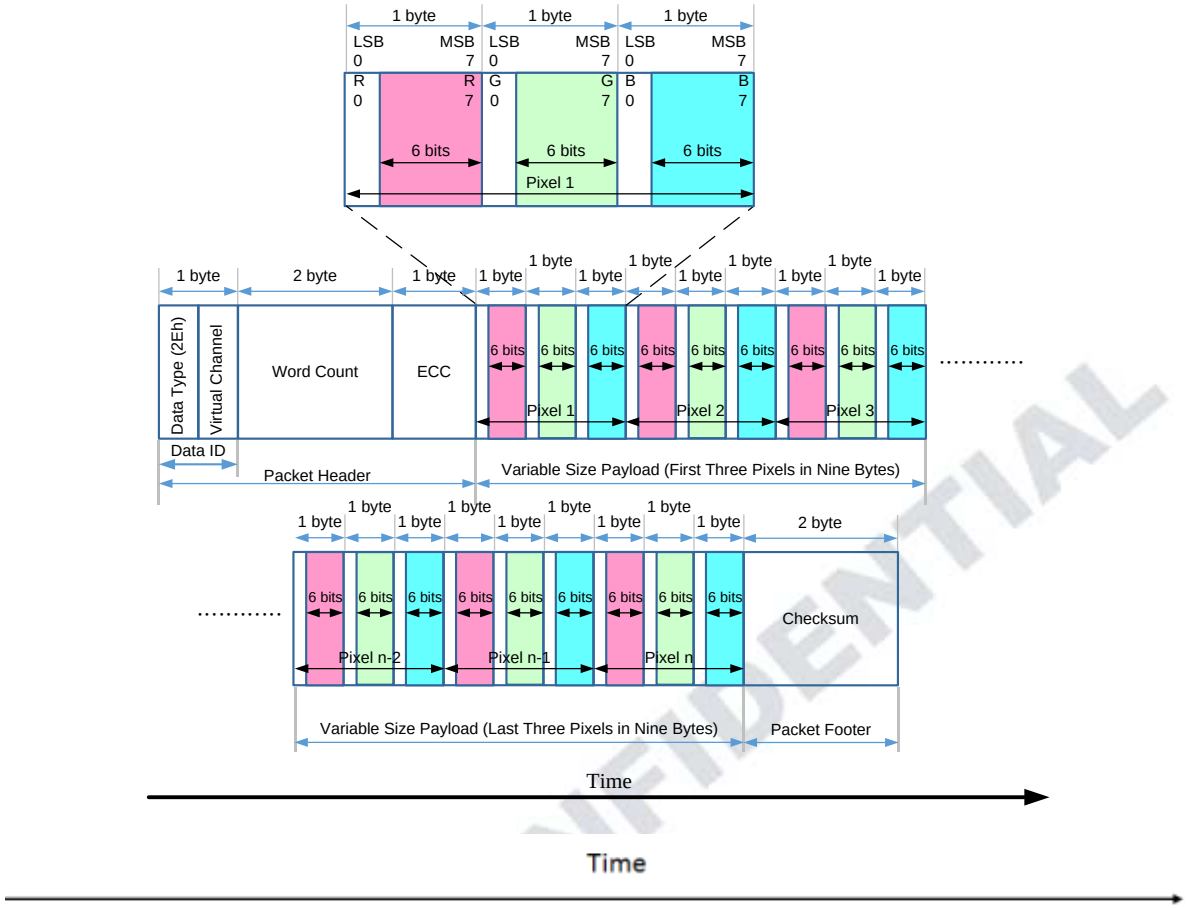


Figure 5-66 18-bit per Pixel (Loosely Packed) – RGB Color Format, Long Packet

In the 18-bit Pixel Loosely Packed format, each R, G, or B color component is six bits but is shifted to the upper bits of the byte, such that the valid pixel bits occupy bits [7:2] of each byte. Bits [1:0] of each payload byte representing active pixels are ignored. As a result, each pixel requires three bytes as it is transmitted across the Link. This requires more bandwidth than the “packed” format, but requires less shifting and multiplexing logic in the packing and unpacking functions on each end of the Link.

This format is used to transmit RGB image data formatted as pixels to a Video Mode display module that displays 18-bit pixels. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (6 bits), green (6 bits) and blue (6 bits) in that order. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

5.7.4 24-bit per Pixel, Long Packet, Data Type 111110 (3Eh)

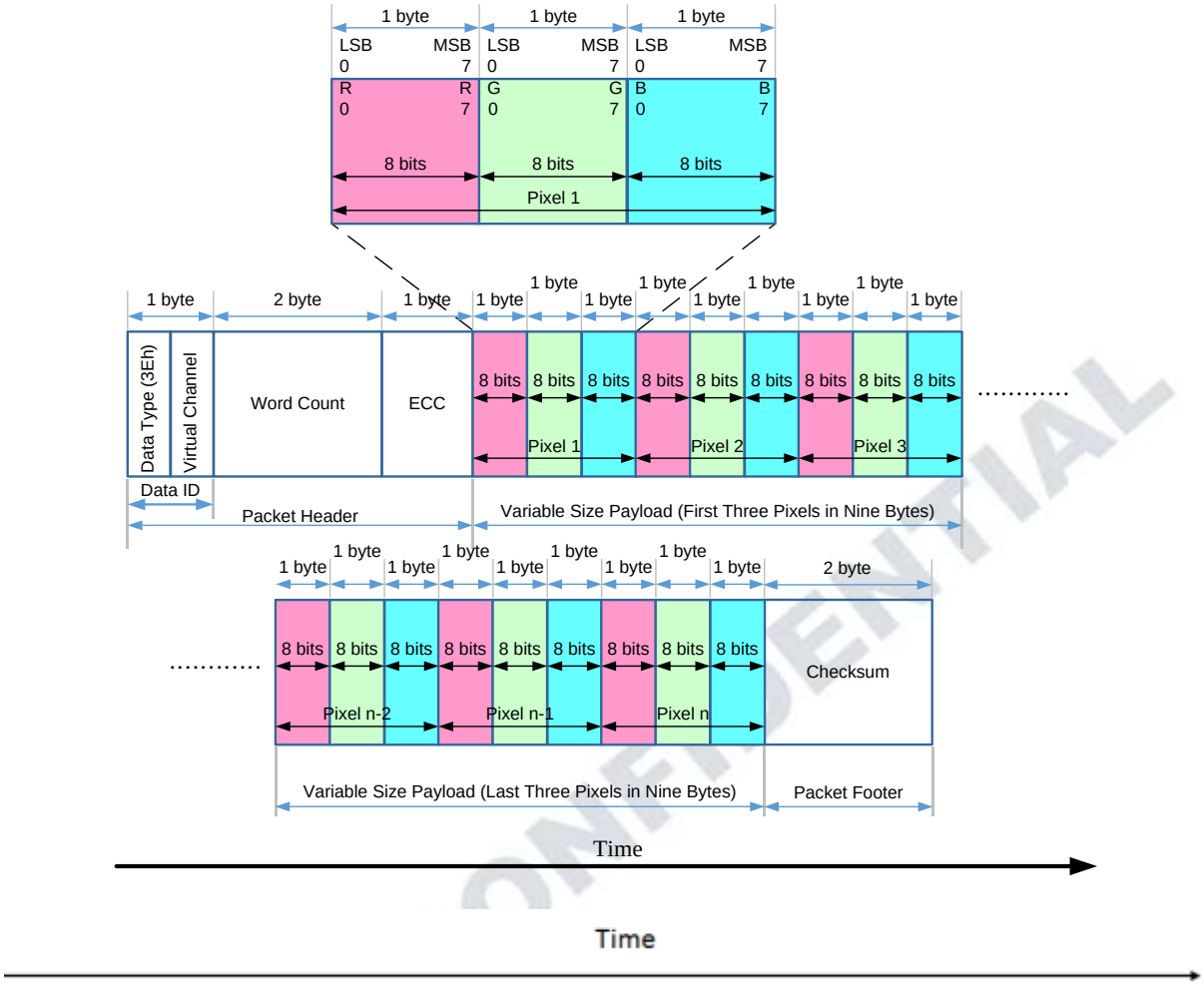


Figure 5-67 24-bit per Pixel – RGB Color Format, Long Packet

Packed Pixel Stream 24-Bit Format is a Long packet. It is used to transmit image data formatted as 24-bit pixels to a Video Mode display module. The packet consists of the DI byte, a two-byte WC, an ECC byte, a payload of length WC bytes and a two-byte Checksum. The pixel format is red (8 bits), green (8 bits) and blue (8 bits), in that order. Each color component occupies one byte in the pixel stream; no components are split across byte boundaries. Within a color component, the LSB is sent first, the MSB last. With this format, pixel boundaries align with byte boundaries every three bytes. The total line width (displayed plus non-displayed pixels) should be a multiple of three bytes.

6. Functions

6.1 Oscillator

The ICNL9707 can oscillate an internal R-C oscillator with an internal oscillation resistor. The oscillation frequency is trimmed according to the internal register. The default frequency setting is 50MHz, and the tolerance of oscillation frequency is ±5%.

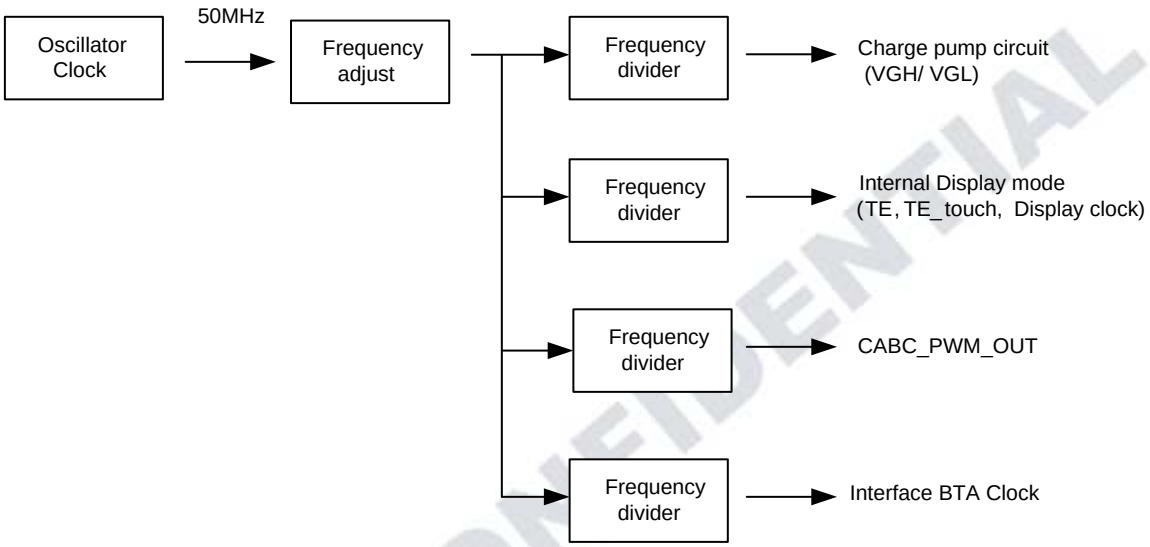


Figure 6-1 Oscillator architecture

6.2 Content Adaptive Brightness Control (CABC)

The CABC, a dynamic backlight control function, drastically reduces the power consumption of the luminance source. The ICNL9707 will refer the gray scale content of the display image to output in PWM waveform then to the LED driver for backlight brightness control. The content of gray scale can be increased while simultaneously lowering the brightness of the backlight to achieve the same perceived brightness. The adjusted gray level scale and the power consumption reduction depend on the content of the image.

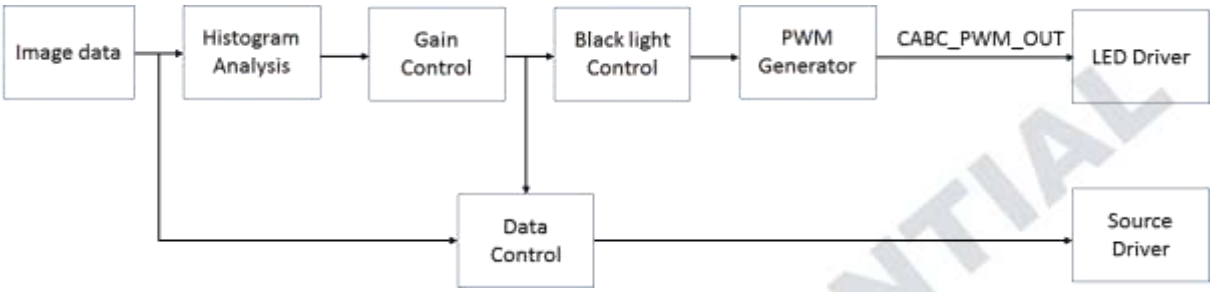


Figure 6-2 CABC Block Diagram

The ICNL9707 can calculate the backlight brightness level and send a CABC_PWM_OUT pulse to the LED driver via CABC_PWM_OUT pin for backlight brightness control purposes. The PWM frequency of 60Hz frame rate application can be adjusted by BCFRQSEL parameters, and the calculating equation is shown below:

$$Number\ of\ PWM\ /\ Frame = (BCFRQSEL + 1) \times 2$$
$$F_{CABC\_PWM\_OUT} = Frame\ rate \times (Num\ of\ PWM\ /\ Frame)_{(Unit:Hz)}$$

The basic timing diagram which is applied from the ICNL9707 in order to control the LED driver.

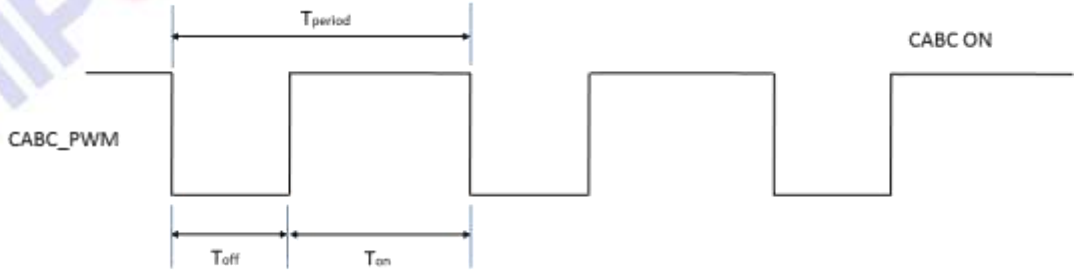
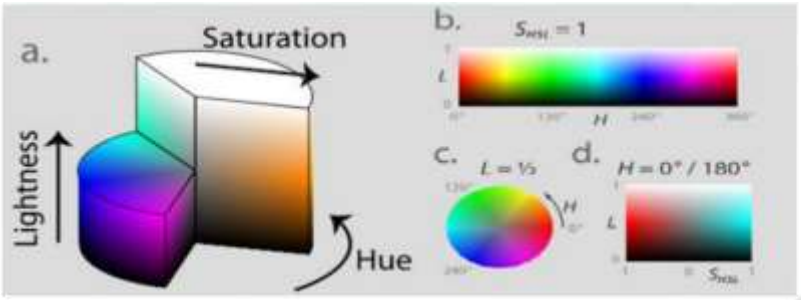


Figure 6-3 CABC_PWM_OUT On/Off Period

6.3 Color Enhancement

CHIPONE's Color Enhancement algorithm provides vivid image process effect, which is provided by three major image process functions: Contrast, Saturation and Sharpness. Each sub-block will be described in the following pages. CHIPONE's Color Enhancement processes image under HSL domain, shown as Figure 6-4, and block diagram is shown in Figure 6-5.



$H \in [0°, 360°]$ *is the angle of the color phase,* $S, L \in [0,1]$ *are the brightness and saturation*

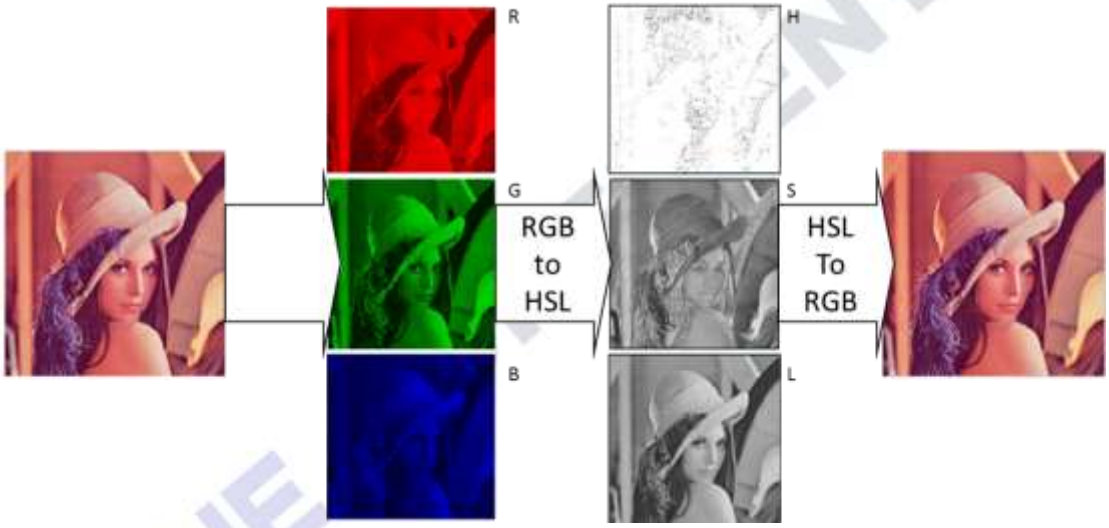


Figure 6-4 RGB to HSL domain

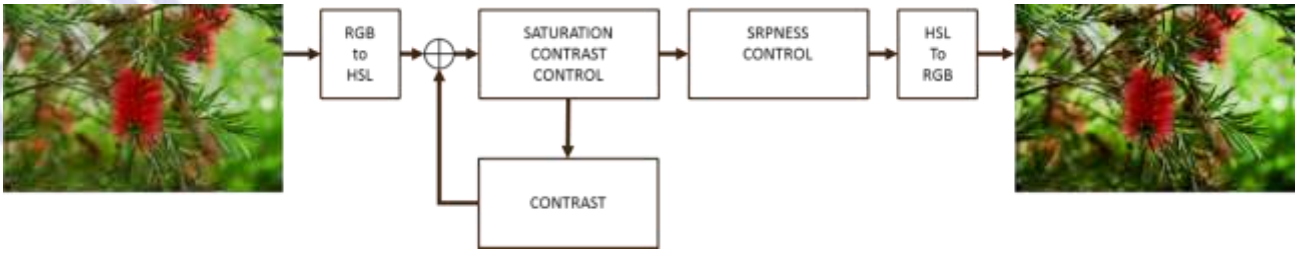


Figure 6-5 CE Block Diagram

6.3.1 Contrast Enhancement

Contrast indicates the clarity of the image content. In CHIPONE's contrast block, it automatically analyzes the input image and process the image specific according to its attribute. And output the picture of better contrast performance.

In Figure 6-6, the original image is all in high gray level, after CHIPONE's contrast process, the image becomes vivid and shows the details.

Figure 6-6 Original image is all in high gray level (Contrast Enhancement)

In Figure 6-7, the original image is too dark and covers too many details. After our contrast process, the contrast of the image improved.

Figure 6-7 Original image is too dark and covers too many details (Contrast Enhancement)

In Figure 6-8 the image has both extremely bright and dark area. After our contrast processing, it keeps the bright part and reappear dark part's details.

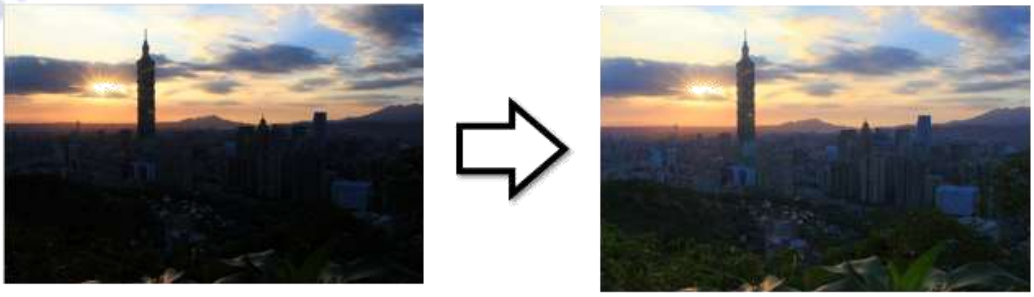


Figure 6-8 Original image has both extremely bright and dark area (Contrast Enhancement)

6.3.2 Saturation Enhancement

CHIPONE's saturation enhancement algorithm can improve the image quality and make color more saturated. We automatically analyze the input image and re-locate the Saturation value according to our designed S-curve to a better degree. Figure 6-9 and Figure 6-10 show our analysis process and the final transformed results.

Figure 6-9 Example 1, Saturation Enhancement

Figure 6-10 Example 2, Saturation Enhancement

6.3.3 Sharpness Enhancement

Sharpness enhancement is an image processing method to sharpen images and generate more readable image. CHIPONE's Sharpness Enhancement function uses high-pass filter to scan the edge and enhance it. Figure 6-11 shows the sharper image compared to the origin one.

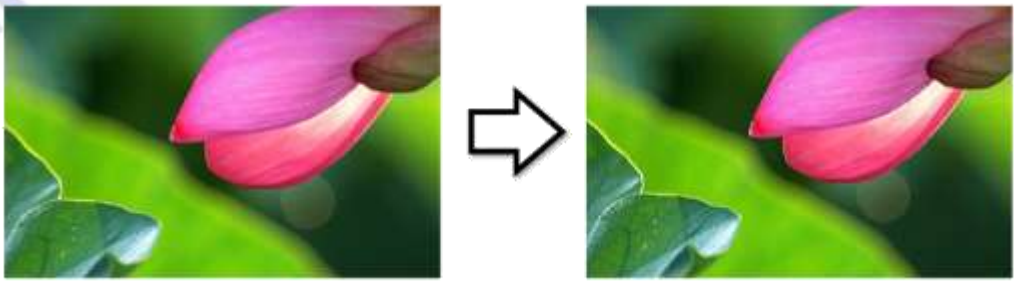


Figure 6-11 Example of Sharpness Enhancement

6.4 Gamma Function

The structure of grayscale amplifier is shown as below figure. ICNL9707 have support separated Gamma Correction function for R/G/B data. There are 19 voltage levels between VGMP/VGMN and Gamma GND (VSSA), which are determined by the reference adjustment register.

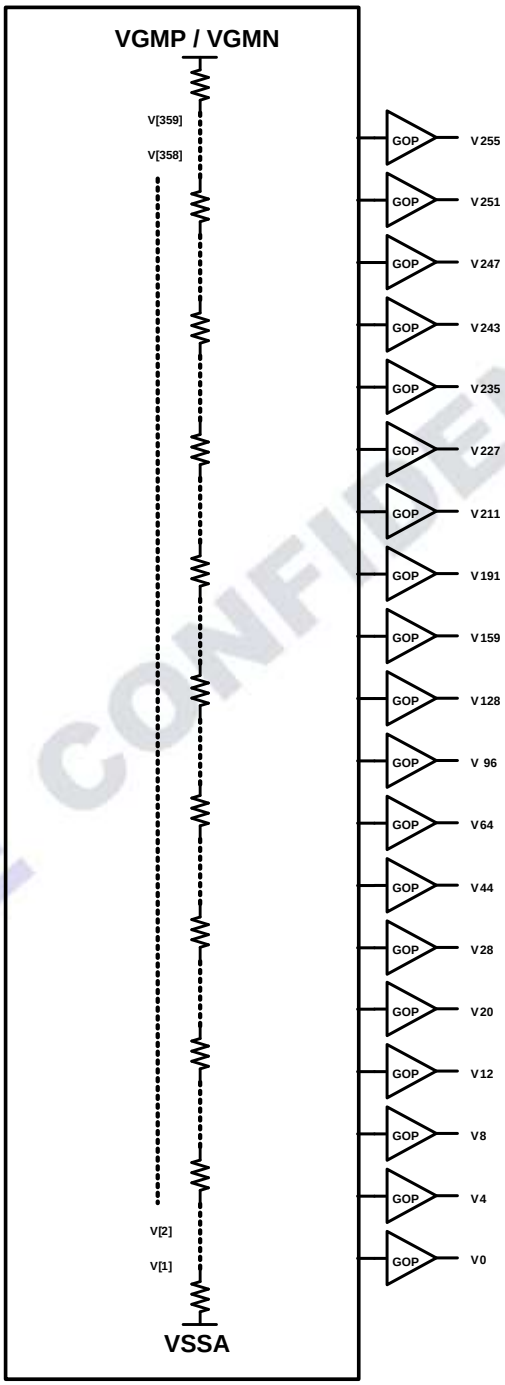


Figure 6-12 Gamma register stream and Gamma reference voltage

6.5 OTP Programing Flow

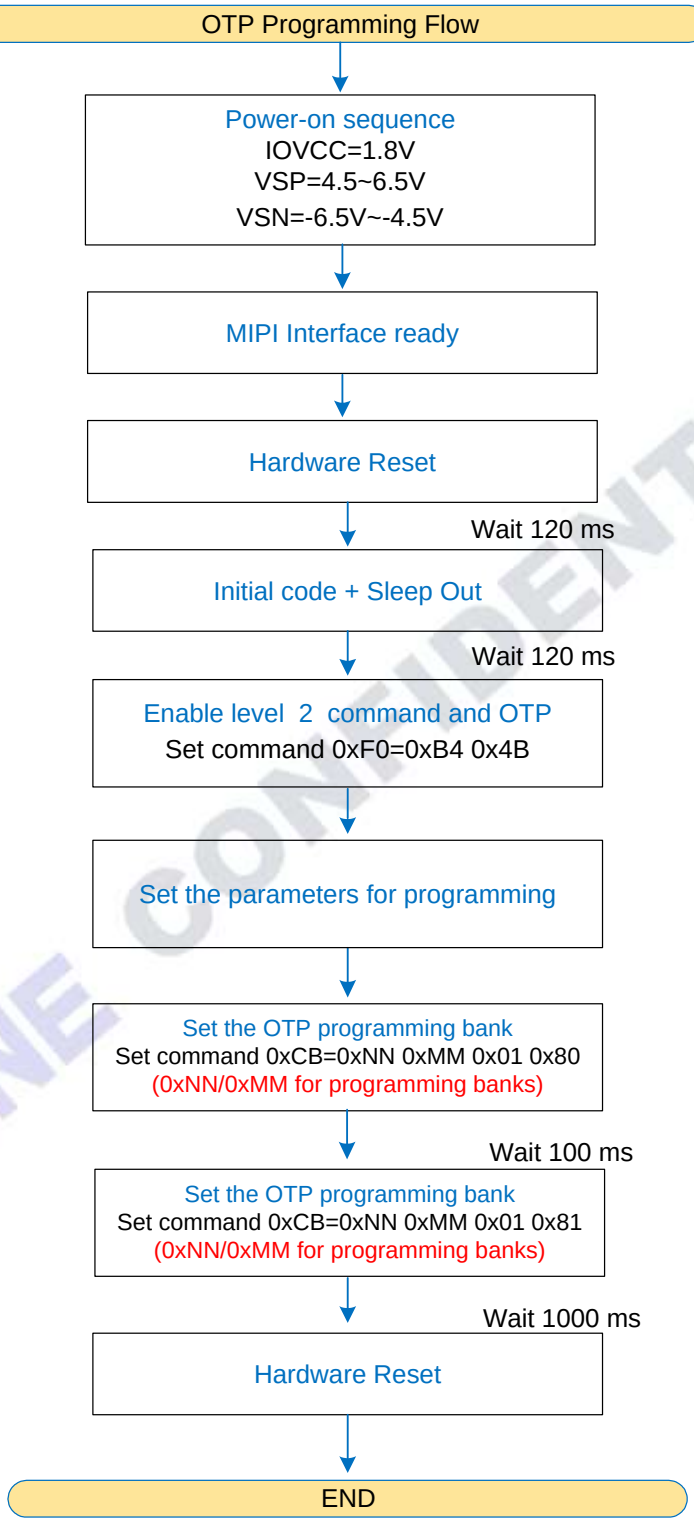


Figure 6-13 OTP Programming Flow

6.6 Tearing Effect

6.6.1 Tearing effect output line

The Tearing Effect output line supplies a panel synchronization signal. This signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect signal is defined by the parameter of the Tearing Effect Line On command. The signal can be used by the MPU to synchronize frame memory writing when displaying video images.
Tearing Effect Line Modes

Mode 1, the Tearing Effect Output signal consists of V-Blanking Information only:

Figure 6-14 Tearing effect output signal mode 1

t_{vdh}= The LCD display is not updated from the Frame Memory

t_{vdl}= The LCD display is updated from the Frame Memory

6.6.2 Tearing effect line timing

The Tearing Effect signal is described below:

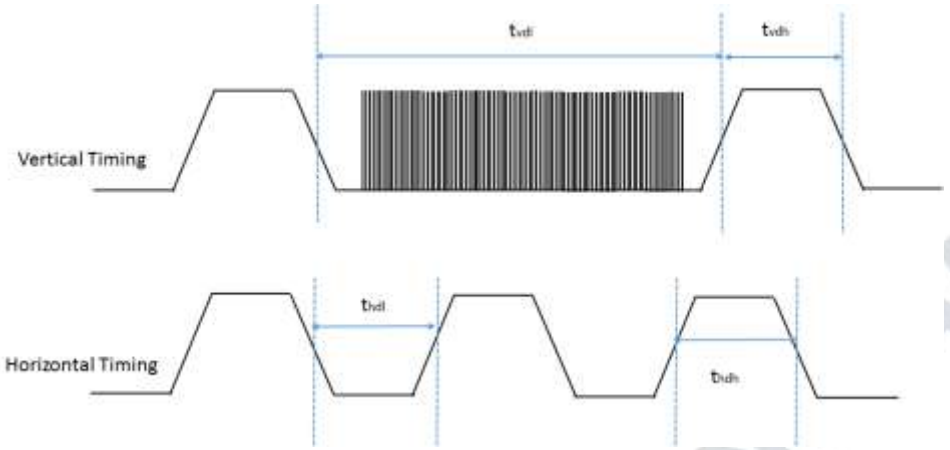


Figure 6-15 Tearing effect output line – tearing effect line timing

Table 6-1 Tearing Effect signal timing

Signal	Symbol	Parameter	Specification			Unit	Notes
			MIN	TYP	MAX		
TE	tvdl	Vertical Timing Low Duration	15			mS	
TE	tvdh	Vertical Timing High Duration	VFP+VBP+VHP			nS	
TE	Tr	Rise Time			15	nS	
TE	Tf	Fall Time			15	nS	

Condition: Idle mode off, Frame Rate =60Hz, Resolution: 1200RGB) *192

Note: MADCTL ML=0 and ML=1

The signal's rise and fall times (T_r, T_f) are stipulated to be equal to or less than 15ns.

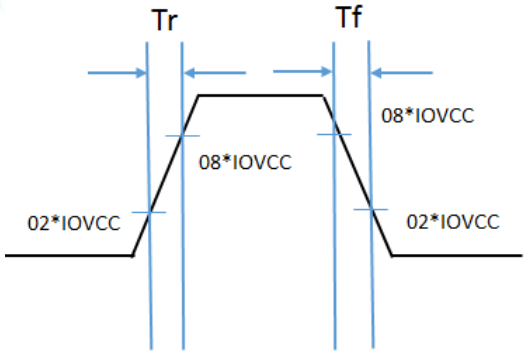


Figure 6-16 Tearing effect output line – definition of Tr,Tf

6.7 Sleep Out – Command

6.7.1 Register loading detection

Sleep-out command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module loading function of factory default values from OTP (or similar device) to registers of the display controller is working properly. There are compared factory values of the OTP and register values of the display controller by the display controller. If those both values (OTP and register values) are same, there is inverted (=increased by 1) a bit, which is defined in command “Read Display Self-Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D7). If those both values are not same, this bit (D7) is not inverted (=increased by 1). The flow chart for this internal function is following:

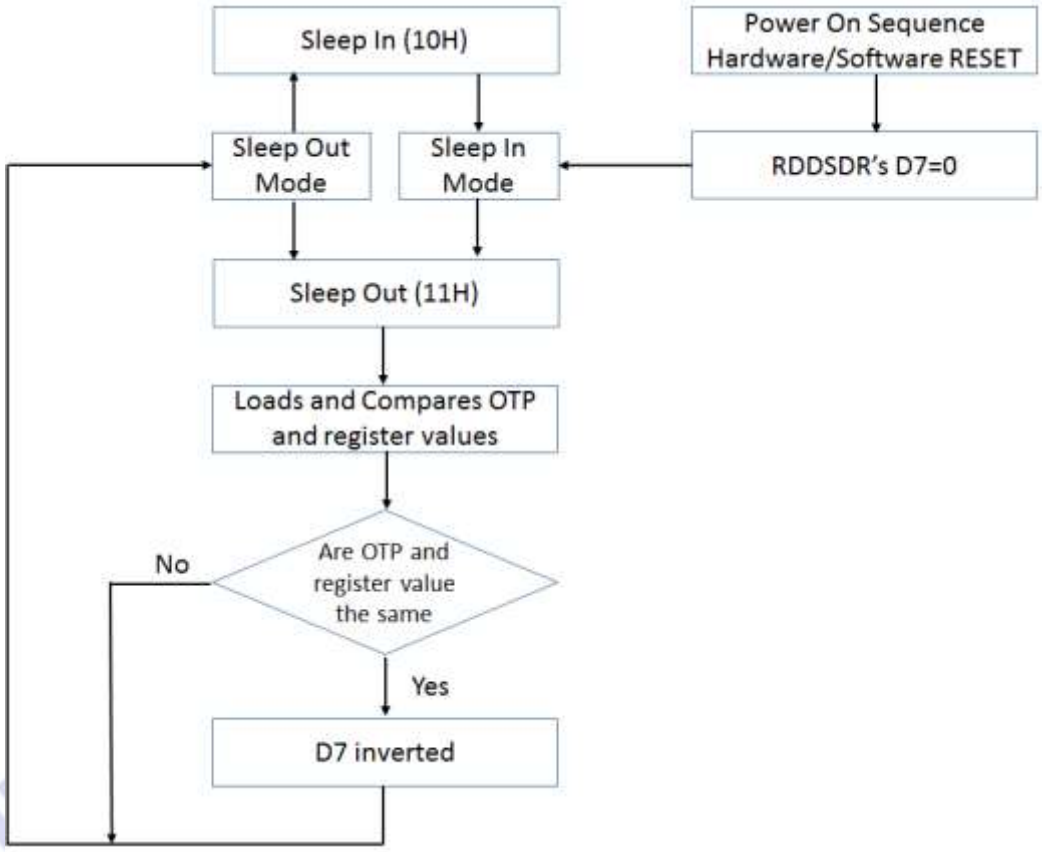


Figure 6-17 Sleep out flow chart-command and self-diagnostic functions

6.7.2 Functionality detection

Sleep Out-command (See “Sleep Out (11h)”) is a trigger for an internal function of the display module, which indicates, if the display module is still running and meets functionality requirements. The internal function (=the display controller) is comparing, if the display module still meets functionality requirements (e.g. booster voltage levels, timings, etc.). If functionality requirement is met, 1 bit will be inverted (=increased by 1), which is defined in command “Read Display Self- Diagnostic Result (0Fh)” (=RDDSDR) (The used bit of this command is D6). If functionality requirement is not the same, this bit (D6) is not inverted (=increased by 1). The flow chart for this internal function is shown as below.

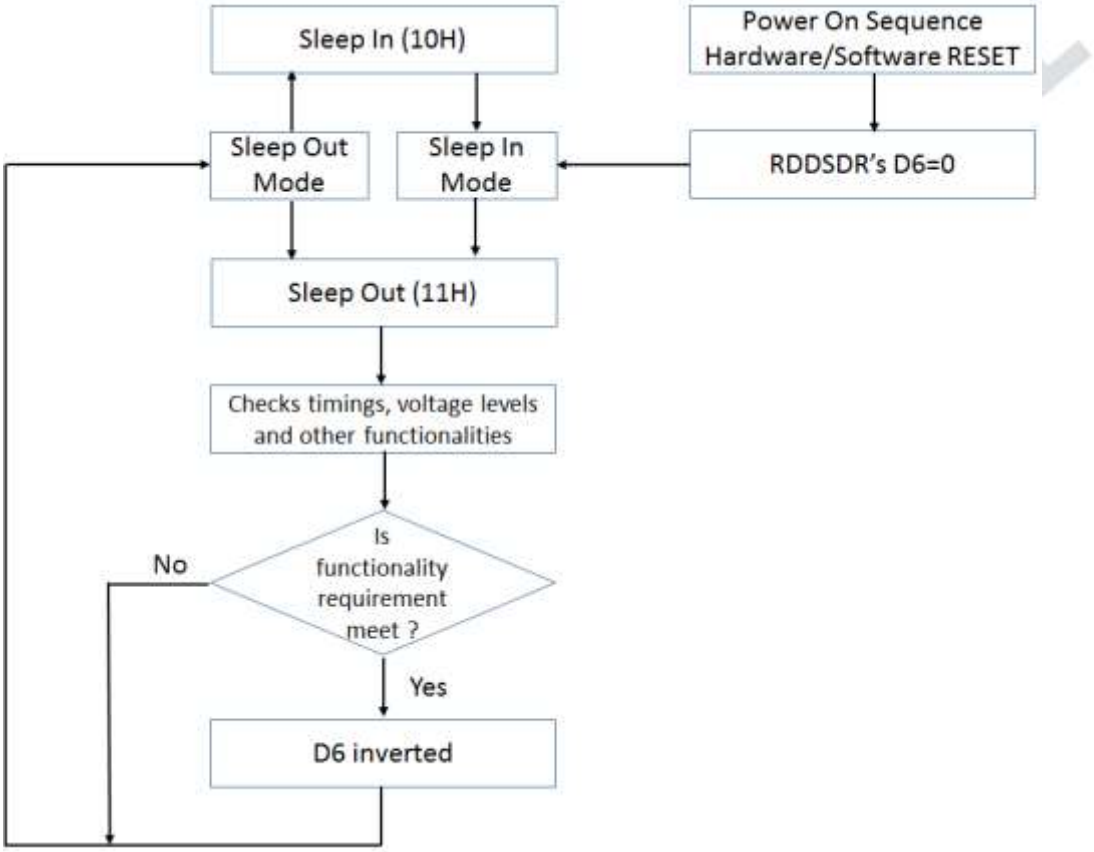


Figure 6-18 Sleep out flow chart internal function detection

Note: There is needed 120msec. After Sleep Out command, when there is changing from sleep In mode to Sleep Out mode, before there is possible to check if Customer’s functionality requirements are met and a value of RDDSDR’s D6 is valid. Otherwise, there is 5msec delay for D6’s value, when Sleep Out command is sent in Sleep Out mode.

7. Power On / OFF Sequence

7.1 Power ON Sequence

Hardware Reset would be applied when power on. The RESX is held at “H” by the host after both VCI and IOVCC have been applied. Otherwise, correct functionality will not be guaranteed. If RESX is held to “L” by the host during Power On, it must keep “L” at least 10μsec after both VCI and IOVCC applied. The power on sequence for different power input modes are shown below.

Table 7-1 Power ON Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T_{on1}	Delay time of IOVCC to VCI	0			ms	
T_{on2}	Delay time of IOVCC to VSP	0			ms	
T1	IOVCC rising time	-		2	ms	
T2	Delay time of IOVCC to valid RESX to “H”	10			ms	
T3	Delay time of RESX “H” to initial code ready	20			ms	
T4	Delay time of IOVCC (HS_VCC) to MIPI bus ready	0		T2	ms	
T5	RESX “L” period	10			us	
T6	Delay time of initial code reloaded to video packet transmit	120			ms	

7.1.1 Power on sequence: PCCS [1:0] = [1,0]

Applied Power: IOVCC, VCI

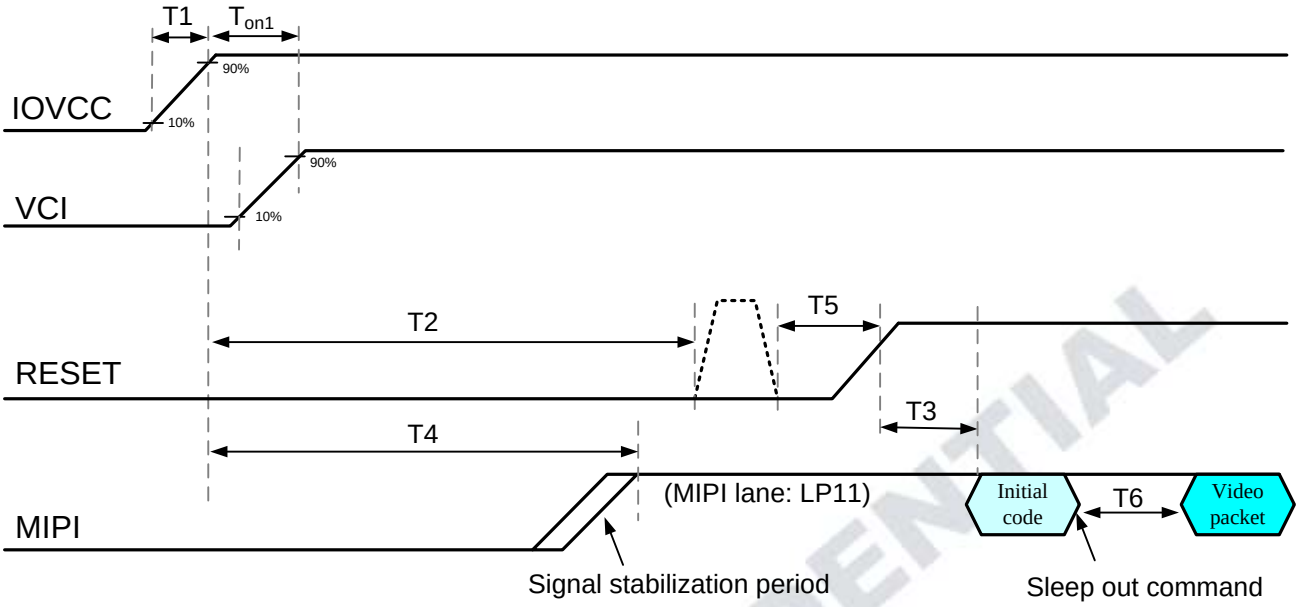


Figure 7-1 Power on sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.1.2 Power on sequence: PCCS [1:0]=[1,1]

Applied Power: IOVCC, VSP, VSN

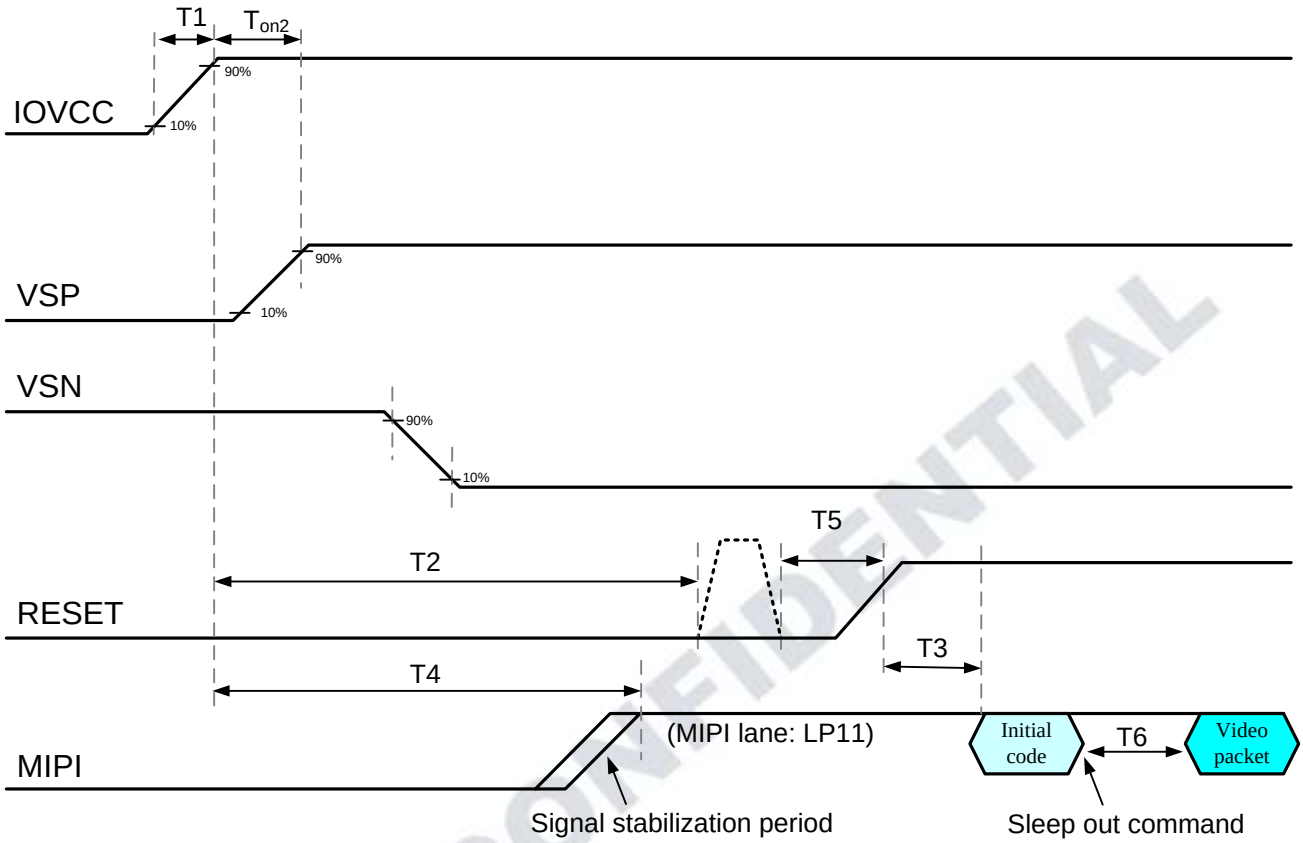


Figure 7-2 Power on sequence at PCCS[1:0]=[1,1] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.2 Power OFF Sequence

Power off sequence for different PCCS-mode applications are shown below:

Table 7-2 Power OFF Sequence Timing

Symbol	Description	Value			Unit	Remark
		Min.	Typ.	Max.		
T_{off1}	Delay time of VCI to IOVCC	0	-	-	ms	
T_{off2}	Delay time of VSP to IOVCC	0	-	-	ms	
T_{off3}	Delay time of VSN to VSP	0	-	-	ms	
T7	IOVCC falling time	-	-	2	ms	
T8	Delay time of RESX “L” to VCI	0	-	-	us	
T9	Delay time of MIPI LP-00 to valid RESX “L”	0	-	-	us	
T10	Delay time of Sleep-in received to valid RESX “L”	100	-	-	ms	
T11	Delay time of RESX “L” to VSN	0	-	-	ms	

7.2.1 Power off sequence: PCCS[1:0] = [1,0]

Application Power: IOVCC, VCI,

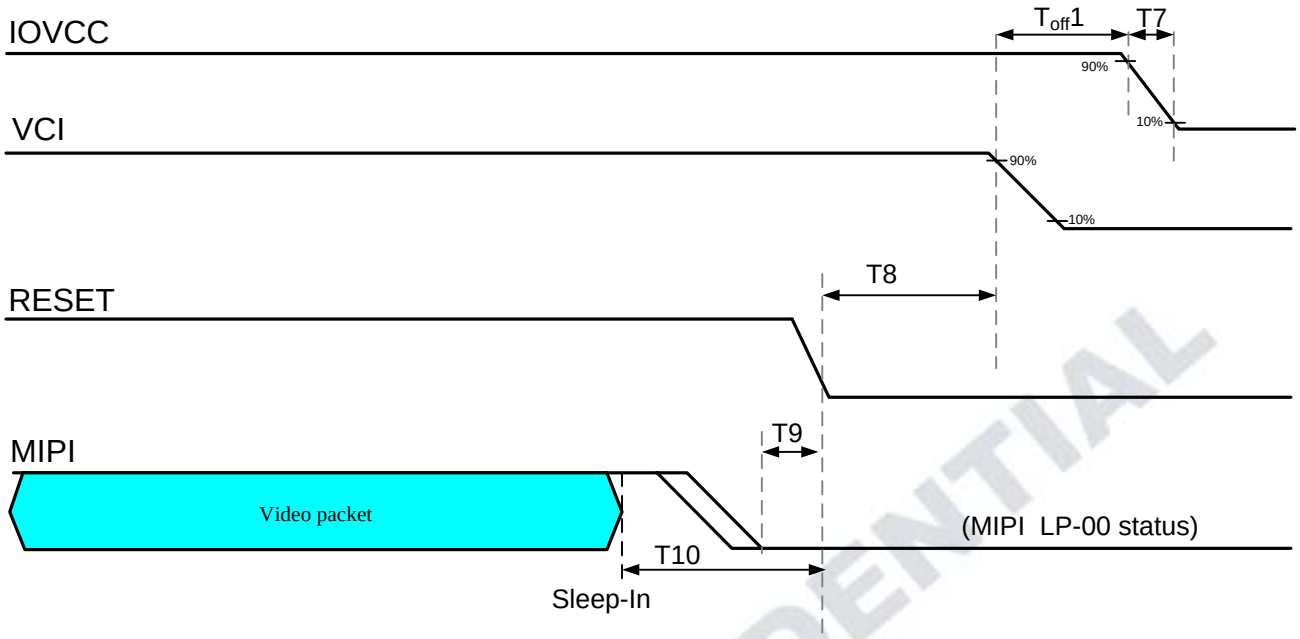


Figure 7-3 Power off sequence at PCCS[1:0]=[1,0] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.2.2 Power off sequence: PCCS[1:0] = [1,1]

Application Power: IOVCC, VSP, VSN

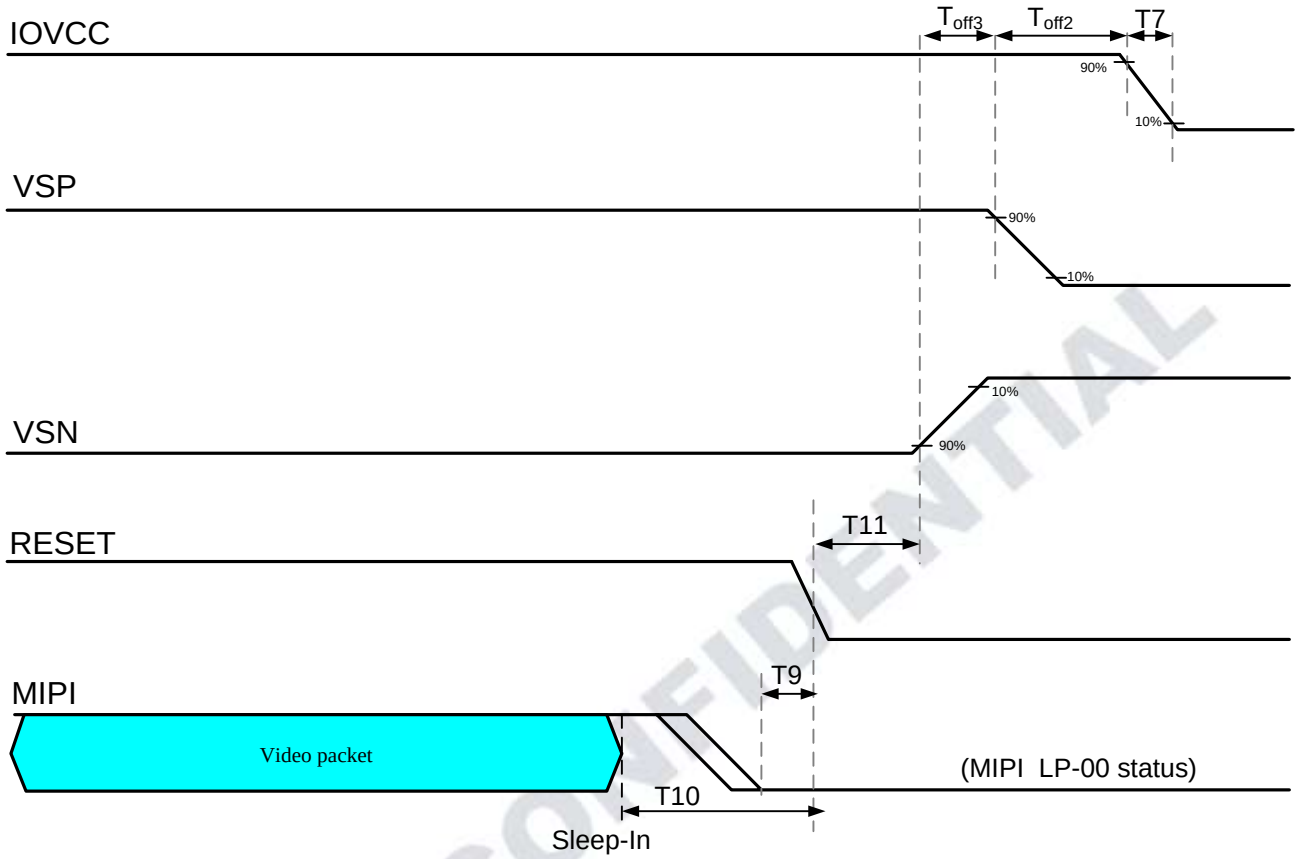


Figure 7-4 Power off sequence at PCCS[1:0]=[1,1] mode

Note1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

8. Command

8.1 Instruction Code Table

8.1.1 Instruction Code Table → Command 1

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
NOP	00h	0	W	No Parameter								-
SWRESET	01h	0	W	No Parameter								-
RDDID	04h	1	R	ID1[7:0]								FFh
		2	R	ID2[7:0]								FFh
		3	R	ID3[7:0]								FFh
RDNUMED	05h	1	R	P[7:0]								00h
RDDST	09h	1	R	ST[31:24]								00h
		2	R	ST[23:16]								71h
		3	R	ST[15:8]								00h
		4	R	ST[7:0]								40h
RDDPM	0Ah	1	R	D[7:0]								08h
RDDMADCTR	0Bh	1	R	D[7:0]								00h
RDDCOLMOD	0Ch	1	R	D[7:0]								70h
RDDIM	0Dh	1	R	D[7:0]								00h
RDDSM	0Eh	1	R	D[7:0]								00h
RDDSDR	0Fh	1	R	D[7:0]								00h
SLPIN	10h	0	W	No Parameter								-
SLPOUT	11h	0	W	No Parameter								-
NORN	13h	0	W	No Parameter								-
INVOFF	20h	0	W	No Parameter								-
INVON	21h	0	W	No Parameter								-
ALLPOFF	22h	0	W	No Parameter								-
ALLPON	23h	0	W	No Parameter								-
GAMSET	26h	1	W	0	0	0	0	GC[3:0]				01h
DISPOFF	28h	0	W	No Parameter								-
DISPON	29h	0	W	No Parameter								-
TEOFF	34h	0	W	No Parameter								-
TEON	35h	1	W	0	0	0	0	0	0	0	M	00h
MADCTR	36h	1	W	0	0	0	ML	RGB	0	MH	0	00h
COLMOD	3Ah	1	W	0	VPF[2:0]			0	0	0	0	70h
STESL	44h	1	W	N[15:8]								00h
		2	W	N[7:0]								00h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
RDSCL	45h	1	R	SLN[15:8]								00h
		2	R	SLN[7:0]								00h
WRDISBV	51h	1	W	-	-	-	-	DBV[11:8]				00h
		2	W	DBV[7:0]								00h
RDDISBV	52h	1	R	-	-	-	-	DBV[11:8]				00h
		2	R	DBV[7:0]								00h
WRCTRLD	53h	1	W	0	0	BCTL	0	DD	BL	0	0	00h
RDCTRLD	54h	1	R	0	0	BCTL	0	DD	BL	0	0	00h
WRCABC	55h	1	W	0	0	0	0	0	0	CABC [1:0]		00h
RDCABC	56h	1	R	0	0	0	0	0	0	CABC [1:0]		00h
WRCABCMB	5Eh	1	R	-	-	-	-	CMB[11:8]				00h
		2	R	CMB[7:0]								00h
RDCABCMB	5Fh	1	R	-	-	-	-	CMB[11:8]				00h
		2	R	CMB[7:0]								00h
Read_DDB_start	A1h	1	R	1	0	0	1	0	1	1	1	97h
		2	R	0	0	0	0	0	0	0	1	01h
		3	R	0	0	0	0	0	0	0	0	00h
		4	R	0	0	0	1	1	0	0	0	18h
Read_DDB_continue	A8h	1	R	-	-	-	-	-	-	-	-	-
		2	R	-	-	-	-	-	-	-	-	-
		3	R	-	-	-	-	-	-	-	-	-
		4	R	-	-	-	-	-	-	-	-	-
RDID1	DAh	1	R	ID1[7:0]								FFh
RDID2	DBh	1	R	ID2[7:0]								FFh
RDID3	DCh	1	R	ID3[7:0]								FFh

8.1.2 Instruction Code Table → Command 2

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
GOUTL	B3h	1	RW	0	0	GOUTL_SEL1[5:0]						03h
		2	RW	0	0	GOUTL_SEL2[5:0]						03h
		3	RW	0	0	GOUTL_SEL3[5:0]						03h
		4	RW	0	0	GOUTL_SEL4[5:0]						03h
		5	RW	0	0	GOUTL_SEL5[5:0]						03h
		6	RW	0	0	GOUTL_SEL6[5:0]						03h
		7	RW	0	0	GOUTL_SEL7[5:0]						03h
		8	RW	0	0	GOUTL_SEL8[5:0]						03h
		9	RW	0	0	GOUTL_SEL9[5:0]						03h
		10	RW	0	0	GOUTL_SEL10[5:0]						03h
		11	RW	0	0	GOUTL_SEL11[5:0]						03h
		12	RW	0	0	GOUTL_SEL12[5:0]						03h
		13	RW	0	0	GOUTL_SEL13[5:0]						03h
		14	RW	0	0	GOUTL_SEL14[5:0]						03h
		15	RW	0	0	GOUTL_SEL15[5:0]						03h
		16	RW	0	0	GOUTL_SEL16[5:0]						03h
		17	RW	0	0	GOUTL_SEL17[5:0]						03h
		18	RW	0	0	GOUTL_SEL18[5:0]						03h
		19	RW	0	0	GOUTL_SEL19[5:0]						03h
		20	RW	0	0	GOUTL_SEL20[5:0]						03h
		21	RW	0	0	GOUTL_SEL21[5:0]						03h
		22	RW	0	0	GOUTL_SEL22[5:0]						03h
GOUTR	B4h	1	RW	0	0	GOUTR_SEL1[5:0]						03h
		2	RW	0	0	GOUTR_SEL2[5:0]						03h
		3	RW	0	0	GOUTR_SEL3[5:0]						03h
		4	RW	0	0	GOUTR_SEL4[5:0]						03h
		5	RW	0	0	GOUTR_SEL5[5:0]						03h
		6	RW	0	0	GOUTR_SEL6[5:0]						03h
		7	RW	0	0	GOUTR_SEL7[5:0]						03h
		8	RW	0	0	GOUTR_SEL8[5:0]						03h
		9	RW	0	0	GOUTR_SEL9[5:0]						03h
		10	RW	0	0	GOUTR_SEL10[5:0]						03h
		11	RW	0	0	GOUTR_SEL11[5:0]						03h
		12	RW	0	0	GOUTR_SEL12[5:0]						03h
		13	RW	0	0	GOUTR_SEL13[5:0]						03h
		14	RW	0	0	GOUTR_SEL14[5:0]						03h
		15	RW	0	0	GOUTR_SEL15[5:0]						03h
		16	RW	0	0	GOUTR_SEL16[5:0]						03h
		17	RW	0	0	GOUTR_SEL17[5:0]						03h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
		18	RW	0	0	GOUTR_SEL18[5:0]						03h
		19	RW	0	0	GOUTR_SEL19[5:0]						03h
		20	RW	0	0	GOUTR_SEL20[5:0]						03h
		21	RW	0	0	GOUTR_SEL21[5:0]						03h
		22	RW	0	0	GOUTR_SEL22[5:0]						03h
SETID	B5h	1	RW	ID1[7:0]								FFh
		2	RW	ID2[7:0]								FFh
		3	RW	ID3[7:0]								FFh
		4	R	0	0	0	0	0	OTP_ID_TIMES[2:0]			00h
PWRCON_VCOM	B6h	1	RW	VCOM_FWS[7:0]								2Fh
		2	RW	VCOM_BWS[7:0]								2Fh
		3	R	0	0	0	0	0	OTP_VCOM_TIMES[2:0]			00h
PWRCON_SEQ	B7h	1	RW	0	0	VSP_DC_H[5:0]						01h
		2	RW	0	0	VSN_DC_H[5:0]						01h
		3	RW	0	0	VCL_DC_H[5:0]						09h
		4	RW	0	0	VGH_DC_H[5:0]						0Dh
		5	RW	0	0	VGL_DC_H[5:0]						11h
		6	RW	0	0	GAM_DC_H[5:0]						19h
		7	RW	0	0	VCOM_DC_H[5:0]						1Dh
		8	RW	0	0	RT_DC_H[5:0]						15h
		9	RW	0	0	0	0	0	0	0	0	00h
		10	RW	0	0	GATE_ON_DC_H[5:0]						25h
		11	RW	0	0	SOFT_L[5:0]						21h
		12	RW	VCL_DC_L[3:0]				VSP_DC_L[3:0]				00h
		13	RW	VCOM_DC_L[3:0]				VGL_DC_L[3:0]				00h
		14	RW	VGH_DC_L[3:0]				VSN_DC_L[3:0]				00h
		15	RW	RT_DC_L[3:0]				GAM_DC_L[3:0]				00h
		16	RW	GATE_ON_DC_L[3:0]				DISCH_L[3:0]				02h
		17	RW	1	1	1	1	0	1	1	1	F7h
		18	RW	0	0	0	1	1	0	0	0	38h
PWRCON_CLK	B8h	1	RW	VCOM_EN_S[1:0]		1	1	DCDC_RT[1:0]		OTP_DCDC_RT[1:0]		34h
		2	RW	0	PWRIC_CLK_S[2:0]			0	0	1	1	53h
		3	RW	0	0	0	0	DCDC_CLK_NS[3:0]				03h
		4	RW	1	1	0	0	1	1	0	0	CCh
PWRCON_BTA	B9h	1	RW	1	0	1	0	0	GAS_VSP_EN	0	1	A5h
		2	RW	0	0	1	0	0	0	0	0	20h
		3	RW	1	1	1	1	1	1	1		FFh
		4	RW	GAS_IO_EN	GAS_IO_S[2:0]			GAS_VSP_S[3:0]				CAh
PWRCON_MODE	Bah	1	RW	VCSW2_HZ	VCSW2_S[2:0]			VCSW1_HZ	VCSW1_S[2:0]			27h
		2	RW	POWERIC_CLK_EN	0	1	1	0	0	1	1	33h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
PWRCON_REG	BDh	1	RW	VDDN_VCOM_S[2:0]			0	0	0	1	1	43h
		2	RW	0	0	0	0	1	1	1	0	0Eh
		3	RW	0	0	0	0	1	1	1	0	0Eh
		4	RW	VGMP_S[7:0]								4Bh
		5	RW	VGMN_S[7:0]								4Bh
		6	RW	0	0	VGH_S[5:0]						14h
		7	RW	0	0	VGL_S[5:0]						14h
		8	RW	0	0	OTP_VGH_S[5:0]						03h
		9	RW	0	1	0	0	0	1	0	0	44h
		10	RW	0	0	0	0	0	0	1	1	03h
BIST	C0h	1	RW	0	0	0	0	0	0	0	BIST_ON	10h
		2	RW	BIST_IMG_SEL[15:8]								FFh
		3	RW	BIST_IMG_SEL[7:0]								FFh
TCON	C1h	1	RW	0	0	VBP[9:8]		0	0	VFP[9:8]		00h
		2	RW	VBP[7:0]								0Ch
		3	RW	VFP[7:0]								10h
		4	RW	VSA[7:0]								04h
		5	RW	0	0	HBP[9:8]		0	0	HFP[9:8]		00h
		6	RW	HBP[7:0]								0Ch
		7	RW	HFP[7:0]								10h
		8	RW	HSA[7:0]								04h
TCON_2	C2h	1	RW	0	0	NL[9:8]		0	RSO[2:0]			20h
		2	RW	NL[7:0]								80h
TCON_3	C3h	1	RW	0	I2O_BLKF_S[2:0]			BLK_KP	O2I_BLKF_S[2:0]			22h
		2	RW	REV_EOR	B4_EOR	B3_EOR	B2_EOR	0	0	0	0	00h
DSTB	C4h	1	R	0	0	0	0	0	0	0	DSTB	00h
SRC_TIM	C6h	1	RW	SD1[7:0]								00h
		2	RW	SD2[7:0]								00h
		3	RW	SD3[7:0]								FFh
		4	RW	1	1	1	1	1	1	1	1	FFh
		5	RW	0	0	0	0	0	0	0	0	00h
		6	RW	1	1	1	1	1	1	1	1	FFh
		7	RW	0	0	0	0	0	0	0	0	00h
		8	RW	0	0	0	0	0	0	0	1	01h
SRCCON	C7h	1	RW	0	1	0	0	0	INV_SEL[2:0]			45h
		2	RW	0	0	1	0	1	0	1	1	2Bh
		3	RW	0	1	0	0	Z_SHIFT	Z_LINE	0	0	41h
		4	RW	PORCH_HIZ	PORCH_GND	SDSW_DATA	SDPORCH_DATA	0	0	0	0	00h
		5	RW	0	0	0	0	0	0	1	0	02h
SET_G	C8h	1	RW	0	P18[6:0]							7Ch

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
AMMA		2	RW	0	P17[6:0]							6Dh
		3	RW	0	P16[6:0]							63h
		4	RW	0	P15[6:0]							59h
		5	RW	0	P14[6:0]							57h
		6	RW	0	P13[6:0]							4Ah
		7	RW	0	P12[6:0]							51h
		8	RW	0	P11[6:0]							3Ah
		9	RW	0	P10[6:0]							55h
		10	RW	0	P9[6:0]							53h
		11	RW	0	P8[6:0]							55h
		12	RW	0	P7[6:0]							7Ah
		13	RW	0	P6[6:0]							6Fh
		14	RW	0	P5[6:0]							7Fh
		15	RW	0	P4[6:0]							75h
		16	RW	0	P3[6:0]							72h
		17	RW	0	P2[6:0]							62h
		18	RW	0	P1[6:0]							2Dh
		19	RW	0	P0[6:0]							06h
		20	RW	0	N18[6:0]							7Ch
		21	RW	0	N17[6:0]							6Dh
		22	RW	0	N16[6:0]							63h
		23	RW	0	N15[6:0]							59h
		24	RW	0	N14[6:0]							57h
		25	RW	0	N13[6:0]							4Ah
		26	RW	0	N12[6:0]							51h
		27	RW	0	N11[6:0]							3Ah
		28	RW	0	N10[6:0]							55h
		29	RW	0	N9[6:0]							53h
		30	RW	0	N8[6:0]							55h
		31	RW	0	N7[6:0]							7Ah
		32	RW	0	N6[6:0]							6Fh
		33	RW	0	N5[6:0]							7Fh
		34	RW	0	N4[6:0]							75h
		35	RW	0	N3[6:0]							72h
		36	RW	0	N2[6:0]							62h
		37	RW	0	N1[6:0]							2Dh
		38	RW	0	N0[6:0]							06h
OTP_AUTO_PROG	CBh	1	RW	OTP_PROG_BANK[7:0]								00h
		2	RW	OTP_PROG_BANK[15:8]								00h
		3	RW	0	0	0	0	0	0	0	OTP_INT_VPP	00h
		4	RW	0	0	0	0	0	0	0	OTP_AUTO_PROG	80h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
ETC	D0h	1	RW	OTP_LD_I2O	OTP_LD_O2O	1	1	BATON_HS	1	1	FS_EN	07h
		2	RW	FS_DETECT[7:0]								10h
		3	RW	BATON_CNT[7:0]								10h
CABC_CTR	E0h	1	RW	0	0	1	1	PWM_POL	0	0	0	30h
		2	RW	0	0	1	0	0	0	0	1	29h
		3	RW	0	0	0	0	0	0	0	0	21h
		4	RW	0	PFSTEP[2:0]			0	DFSTEP[2:0]			10h
		5	RW	0	0	PWMSTEP[5:0]						1Fh
		6	RW	0	0	0	0	0	1	1	0	06h
		7	RW	0	1	1	0	0	0	1	0	62h
		8	RW	0	DBV_SEL	0	1	1	1	1	1	1Fh
		9	RW	1	0	1	0	0	0	0	0	A0h
		10	RW	DATASTEP[3:0]				0	1	0	0	14h
		11	RW	1	1	0	0	1	1	0	0	CCh
		12	RW	0	0	0	0	0	0	0	0	00h
		13	RW	TGN0_00 [[7:0]								FFh
		14	RW	TGN0_02 [7:0]								FAh
		15	RW	TGN0_03 [7:0]								FDh
		16	RW	TGN0_04 [7:0]								F0h
		17	RW	TGN0_05 [7:0]								FDh
		18	RW	TGN0_06 [7:0]								F8h
		19	RW	TGN0_07 [7:0]								FDh
		20	RW	TGN0_08 [7:0]								F8h
		21	RW	TGN0_09 [7:0]								FAh
		22	RW	TGN0_10 [1:0]								FCh
		23	RW	TGN0_11 [7:0]								FCh
		24	RW	TGN0_12 [7:0]								F0h
		25	RW	TGN0_13 [7:0]								FFh
CABC_SET_1	E1h	1	RW	TGN1_00 [7:0]								AFh
		2	RW	TGN1_01 [7:0]								C8h
		3	RW	TGN1_02 [7:0]								EAh
		4	RW	TGN1_03 [7:0]								E6h
		5	RW	TGN1_04 [7:0]								E4h
		6	RW	TGN1_05 [7:0]								CCh
		7	RW	TGN1_06 [7:0]								E4h
		8	RW	TGN1_07 [7:0]								BEh
		9	RW	TGN1_08 [7:0]								F0h
		10	RW	TGN1_09 [7:0]								B2h
		11	RW	TGN1_10 [7:0]								BEh
		12	RW	TGN1_11 [7:0]								C6h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
		13	RW	TGN1_12 [7:0]								FFh
		14	RW	TGN2_00 [7:0]								AFh
		15	RW	TGN2_01 [7:0]								C8h
		16	RW	TGN2_02 [7:0]								E9h
		17	RW	TGN2_03 [7:0]								E5h
		18	RW	TGN2_04 [7:0]								E3h
		19	RW	TGN2_05 [7:0]								CBh
		20	RW	TGN2_06 [7:0]								E3h
		21	RW	TGN2_07 [7:0]								BEh
		22	RW	TGN2_08 [7:0]								EFh
		23	RW	TGN2_09 [7:0]								B2h
		24	RW	TGN2_10 [7:0]								BEh
		25	RW	TGN2_11 [7:0]								C6h
		26	RW	TGN2_12 [7:0]								FFh
CABCP WM_SET_1	E2h	1	RW	BCRECY0_01[11:8]				BCRECY0_00[11:8]				EFh
		2	RW	BCRECY0_03[11:8]				BCRECY0_02[11:8]				EFh
		3	RW	BCRECY0_05[11:8]				BCRECY0_04[11:8]				EFh
		4	RW	BCRECY0_07[11:8]				BCRECY0_06[11:8]				EFh
		5	RW	BCRECY0_09[11:8]				BCRECY0_08[11:8]				EFh
		6	RW	BCRECY0_11[11:8]				BCRECY0_10[11:8]				EFh
		7	RW	0	0	0	0	BCRECY0_12[11:8]				0Fh
		8	RW	BCRECY0_00[7:0]								80h
		9	RW	BCRECY0_01[7:0]								D0h
		10	RW	BCRECY0_02[7:0]								00h
		11	RW	BCRECY0_03[7:0]								00h
		12	RW	BCRECY0_04[7:0]								00h
		13	RW	BCRECY0_05[7:0]								C0h
		14	RW	BCRECY0_06[7:0]								00h
		15	RW	BCRECY0_07[7:0]								C0h
		16	RW	BCRECY0_08[7:0]								00h
		17	RW	BCRECY0_09[7:0]								F0h
		18	RW	BCRECY0_10[7:0]								F0h
		19	RW	BCRECY0_11[7:0]								00h
		20	RW	BCRECY0_12[7:0]								80h
CABCP WM_SET_2	E3h	1	RW	BCRECY1_01[11:8]				BCRECY1_00[11:8]				98h
		2	RW	BCRECY1_03[11:8]				BCRECY1_02[11:8]				9Eh
		3	RW	BCRECY1_05[11:8]				BCRECY1_04[11:8]				BCh
		4	RW	BCRECY1_07[11:8]				BCRECY1_06[11:8]				ACh
		5	RW	BCRECY1_09[11:8]				BCRECY1_08[11:8]				9Bh
		6	RW	BCRECY1_11[11:8]				BCRECY1_10[11:8]				79h
		7	RW	0	0	0	0	BCRECY1_12[11:8]				0Fh

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
		8	RW	BCRECY1_00[7:0]								F0h
		9	RW	BCRECY1_01[7:0]								80h
		10	RW	BCRECY1_02[7:0]								30h
		11	RW	BCRECY1_03[7:0]								00h
		12	RW	BCRECY1_04[7:0]								80h
		13	RW	BCRECY1_05[7:0]								00h
		14	RW	BCRECY1_06[7:0]								80h
		15	RW	BCRECY1_07[7:0]								00h
		16	RW	BCRECY1_08[7:0]								E0h
		17	RW	BCRECY1_09[7:0]								60h
		18	RW	BCRECY1_10[7:0]								60h
		19	RW	BCRECY1_11[7:0]								FFh
		20	RW	BCRECY1_12[7:0]								D0h
CABCP WM_SE T_3	E4h	1	RW	BCRECY2_01[11:8]				BCRECY2_00[11:8]				98h
		2	RW	BCRECY2_03[11:8]				BCRECY2_02[11:8]				8Eh
		3	RW	BCRECY2_05[11:8]				BCRECY2_04[11:8]				ACh
		4	RW	BCRECY2_07[11:8]				BCRECY2_06[11:8]				ACh
		5	RW	BCRECY2_09[11:8]				BCRECY2_08[11:8]				9Bh
		6	RW	BCRECY2_11[11:8]				BCRECY2_10[11:8]				79h
		7	RW	0	0	0	0	BCRECY2_12[11:8]				0Fh
		8	RW	BCRECY2_00[7:0]								E0h
		9	RW	BCRECY2_01[7:0]								70h
		10	RW	BCRECY2_02[7:0]								20h
		11	RW	BCRECY2_03[7:0]								F0h
		12	RW	BCRECY2_04[7:0]								70h
		13	RW	BCRECY2_05[7:0]								F0h
		14	RW	BCRECY2_06[7:0]								70h
		15	RW	BCRECY2_07[7:0]								00h
		16	RW	BCRECY2_08[7:0]								D0h
		17	RW	BCRECY2_09[7:0]								60h
		18	RW	BCRECY2_10[7:0]								50h
		19	RW	BCRECY2_11[7:0]								FFh
		20	RW	BCRECY2_12[7:0]								C0h
CE_SET	E5h	1	RW	0	0	CONST _ON	SKIN_O N	0	SE_ON	HP_ON	0	00h
		2	RW	0	0	0	1	0	0	1	0	12h
		3	RW	0	0	0	0	1	1	1	1	0Fh
		4	RW	1	1	1	1	1	1	1	1	FFh
		5	RW	1	1	1	1	1	1	1	1	FFh
		6	RW	1	1	1	1	1	1	1	1	FFh
		7	RW	0	0	0	0	0	0	0	0	00h
		8	RW	0	0	0	0	0	0	0	0	00h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
DGC_CTRL	E7h	1	RW	0	0	0	0	0	0	DTR_EN	DGC_EN	00h
DGC_R	E8h	1	RW	DGC_R_V255[9:2]								FFh
		2	RW	DGC_R_V254[9:2]								FEh
		3	RW	DGC_R_V252[9:2]								FCh
		4	RW	DGC_R_V250[9:2]								FAh
		5	RW	DGC_R_V248[9:2]								F8h
		6	RW	DGC_R_V244[9:2]								F4h
		7	RW	DGC_R_V240[9:2]								F0h
		8	RW	DGC_R_V232[9:2]								E8h
		9	RW	DGC_R_V224[9:2]								E0h
		10	RW	DGC_R_V208[9:2]								D0h
		11	RW	DGC_R_V192[9:2]								C0h
		12	RW	DGC_R_V160[9:2]								A0h
		13	RW	DGC_R_V128[9:2]								80h
		14	RW	DGC_R_V127[9:2]								7Fh
		15	RW	DGC_R_V95[9:2]								5Fh
		16	RW	DGC_R_V63[9:2]								3Fh
		17	RW	DGC_R_V47[9:2]								2Fh
		18	RW	DGC_R_V31[9:2]								1Fh
		19	RW	DGC_R_V23[9:2]								17h
		20	RW	DGC_R_V15[9:2]								0Fh
		21	RW	DGC_R_V11[9:2]								0Bh
		22	RW	DGC_R_V7[9:2]								07h
		23	RW	DGC_R_V5[9:2]								05h
		24	RW	DGC_R_V3[9:2]								03h
		25	RW	DGC_R_V1[9:2]								01h
		26	RW	DGC_R_V0[9:2]								00h
DGC_G	E9h	1	RW	DGC_G_V255[9:2]								FFh
		2	RW	DGC_G_V254[9:2]								FEh
		3	RW	DGC_G_V252[9:2]								FCh
		4	RW	DGC_G_V250[9:2]								FAh
		5	RW	DGC_G_V248[9:2]								F8h
		6	RW	DGC_G_V244[9:2]								F4h
		7	RW	DGC_G_V240[9:2]								F0h
		8	RW	DGC_G_V232[9:2]								E8h
		9	RW	DGC_G_V224[9:2]								E0h
		10	RW	DGC_G_V208[9:2]								D0h
		11	RW	DGC_G_V192[9:2]								C0h
		12	RW	DGC_G_V160[9:2]								A0h
		13	RW	DGC_G_V128[9:2]								80h

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
		14	RW	DGC_G_V127[9:2]								7Fh
		15	RW	DGC_G_V95[9:2]								5Fh
		16	RW	DGC_G_V63[9:2]								3Fh
		17	RW	DGC_G_V47[9:2]								2Fh
		18	RW	DGC_G_V31[9:2]								1Fh
		19	RW	DGC_G_V23[9:2]								17h
		20	RW	DGC_G_V15[9:2]								0Fh
		21	RW	DGC_G_V11[9:2]								0Bh
		22	RW	DGC_G_V7[9:2]								07h
		23	RW	DGC_G_V5[9:2]								05h
		24	RW	DGC_G_V3[9:2]								03h
		25	RW	DGC_G_V1[9:2]								01h
		26	RW	DGC_G_V0[9:2]								00h
DGC_B	EAh	1	RW	DGC_B_V255[9:2]								OFF
		2	RW	DGC_B_V254[9:2]								FEh
		3	RW	DGC_B_V252[9:2]								FCh
		4	RW	DGC_B_V250[9:2]								FAh
		5	RW	DGC_B_V248[9:2]								F8h
		6	RW	DGC_B_V244[9:2]								F4h
		7	RW	DGC_B_V240[9:2]								F0h
		8	RW	DGC_B_V232[9:2]								E8h
		9	RW	DGC_B_V224[9:2]								E0h
		10	RW	DGC_B_V208[9:2]								D0h
		11	RW	DGC_B_V192[9:2]								C0h
		12	RW	DGC_B_V160[9:2]								A0h
		13	RW	DGC_B_V128[9:2]								80h
		14	RW	DGC_B_V127[9:2]								7Fh
		15	RW	DGC_B_V95[9:2]								5Fh
		16	RW	DGC_B_V63[9:2]								3Fh
		17	RW	DGC_B_V47[9:2]								2Fh
		18	RW	DGC_B_V31[9:2]								1Fh
		19	RW	DGC_B_V23[9:2]								17h
		20	RW	DGC_B_V15[9:2]								0Fh
		21	RW	DGC_B_V11[9:2]								0Bh
		22	RW	DGC_B_V7[9:2]								07h
		23	RW	DGC_B_V5[9:2]								05h
		24	RW	DGC_B_V3[9:2]								03h
		25	RW	DGC_B_V1[9:2]								01h
		26	RW	DGC_B_V0[9:2]								00h
DGC_R_L	EBh	1	RW	DGC_R_V255[1:0]			DGC_R_V254[1:0]			DGC_R_V252[1:0]		00h
		2	RW	DGC_R_V248[1:0]			DGC_R_V244[1:0]			DGC_R_V240[1:0]		00hh

Name	CMD	Para	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial
		3	RW	DGC_R_V224[1:0]		DGC_R_V208[1:0]		DGC_R_V192[1:0]		DGC_R_V160[1:0]		00h
		4	RW	DGC_R_V128[1:0]		DGC_R_V127[1:0]		DGC_R_V95[1:0]		DGC_R_V63[1:0]		00h
		5	RW	DGC_R_V47[1:0]		DGC_R_V31[1:0]		DGC_R_V23[1:0]		DGC_R_V15[1:0]		00h
		6	RW	DGC_R_V11[1:0]		DGC_R_V7[1:0]		DGC_R_V5[1:0]		DGC_R_V3[1:0]		00h
		7	RW	DGC_R_V1[1:0]		DGC_R_V0[1:0]		0	0	0	0	00h
DGC_G_L	ECh	1	RW	DGC_G_V255[1:0]		DGC_G_V254[1:0]		DGC_G_V252[1:0]		DGC_G_V250[1:0]		00h
		2	RW	DGC_G_V248[1:0]		DGC_G_V244[1:0]		DGC_G_V240[1:0]		DGC_G_V232[1:0]		00h
		3	RW	DGC_G_V224[1:0]		DGC_G_V208[1:0]		DGC_G_V192[1:0]		DGC_G_V160[1:0]		00h
		4	RW	DGC_G_V128[1:0]		DGC_G_V127[1:0]		DGC_G_V95[1:0]		DGC_G_V63[1:0]		00h
		5	RW	DGC_G_V47[1:0]		DGC_G_V31[1:0]		DGC_G_V23[1:0]		DGC_G_V15[1:0]		00h
		6	RW	DGC_G_V11[1:0]		DGC_G_V7[1:0]		DGC_G_V5[1:0]		DGC_G_V3[1:0]		00h
		7	RW	DGC_G_V1[1:0]		DGC_G_V0[1:0]		0	0	0	0	00h
DGC_B_L	EDh	1	RW	DGC_B_V255[1:0]		DGC_B_V254[1:0]		DGC_B_V252[1:0]		DGC_B_V250[1:0]		00h
		2	RW	DGC_B_V248[1:0]		DGC_B_V244[1:0]		DGC_B_V240[1:0]		DGC_B_V232[1:0]		00h
		3	RW	DGC_B_V224[1:0]		DGC_B_V208[1:0]		DGC_B_V192[1:0]		DGC_B_V160[1:0]		00h
		4	RW	DGC_B_V128[1:0]		DGC_B_V127[1:0]		DGC_B_V95[1:0]		DGC_B_V63[1:0]		00h
		5	RW	DGC_B_V47[1:0]		DGC_B_V31[1:0]		DGC_B_V23[1:0]		DGC_B_V15[1:0]		00h
		6	RW	DGC_B_V11[1:0]		DGC_B_V7[1:0]		DGC_B_V5[1:0]		DGC_B_V3[1:0]		00h
		7	RW	DGC_B_V1[1:0]		DGC_B_V0[1:0]		0	0	0	0	00h

8.2 Command 1 description

8.2.1 NOP: NOP (00h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NOP	W	0	0	0	0	0	0	0	0	00h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description	This command is empty command. It does not have effect on the display module.
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / N/A S/W Reset / N/A H/W Reset / N/A
Flow Chart	-

8.2.2 SWRESET: Software Reset (01h)

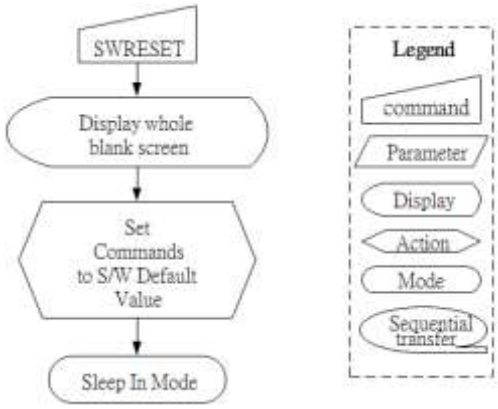
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SWRESET	W	0	0	0	0	0	0	0	1	01h
Parameter		No Parameter								

***NOTE**: "-"Don't care*

Description	When the Software Reset command is written, it causes a software reset. It resets the commands and parameters to their S/W Reset default values and all source & gate outputs are set to GND (display off).
Restriction	It will be necessary to wait 5msec before sending new command following software reset. The display module loads all display suppliers' factory default values to the registers during 5msec. If Software Reset is applied during Sleep Out mode, it will be necessary to wait 120msec before sending Sleep Out command. Software Reset command cannot be sent during Sleep Out sequence.
Register Availability	
Default	
Flow Chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Status	Default Value
Power On Sequence	N/A
S/W Reset	N/A
H/W Reset	N/A



8.2.3 RDDID: Read Display ID (04h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDID	R	0	0	0	0	0	1	0	0	04h
Parameter	1	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10	FFh
Parameter	2	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20	FFh
Parameter	3	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30	FFh

***NOTE**: "-"Don't care*

Description

This read byte returns 24-bit display identification information.

The 1st (ID17 to ID10): LCD module's manufacturer ID.

The 2nd parameter (ID27 to ID20): LCD module/driver version ID.

The 3rd parameter (ID37 to UD30): LCD module/driver ID.

***NOTE**: Commands RDID1/2/3(DAh, DBh, DCh) read data correspond to the parameters 1, 2 and 3 of the command 04h, respectively.

Restriction

-

Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

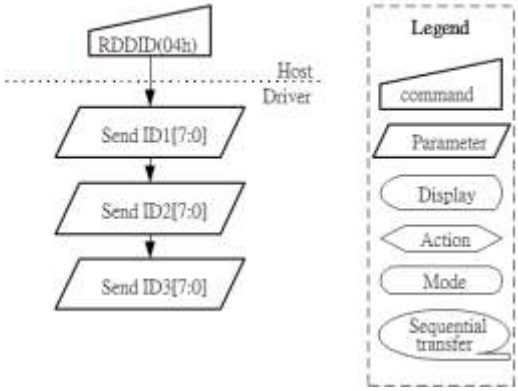
Default

If ID1/ID2/ID3 OTP are not yet programmed:

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	00h	80h	00h
S/W Reset	00h	80h	00h
H/W Reset	00h	80h	00h

If ID1/ID2/ID3 OTP were programmed:

Status	Default Value		
	ID1	ID2	ID3
Power On Sequence	(OTP value)	(OTP value)	(OTP value)
S/W Reset	(OTP value)	(OTP value)	(OTP value)
H/W Reset	(OTP value)	(OTP value)	(OTP value)

Flow Chart	

8.2.4 RDNUMED: Read Number of Errors on DSI (05h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDNUMED	R	0	0	0	0	0	1	0	1	05h
Parameter	1	P7	P6	P5	P4	P3	P2	P1	P0	00h

***NOTE**: "-"Don't care*

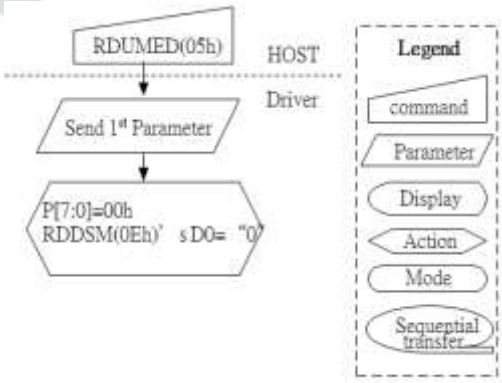
Description	The first parameter is telling a number of the parity errors on DSI. The more detailed description of the bits is below. P[6..0] bits are telling a number of the parity errors. P[7] is set to "1" if there is overflow with P[6..0] bits. P[7..0] bits are set to "0"s (as well as RDDSM(0Eh)'s D0 are set "0" at the same time) after there is sent the first parameter information (= The read function is completed). See also section "Acknowledge with Error Report (AwER)" and command RDDSM 0Eh.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	No Changed
H/W Reset	00h

Flow Chart



8.2.5 RDDST: Read Display Status (09h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDST	R	0	0	0	0	1	0	0	1	09h
Parameter	1	ST31	ST30	ST29	ST28	ST27	ST26	ST25	ST24	00h
Parameter	2	ST23	ST22	ST21	ST20	ST19	ST18	ST17	ST16	71h
Parameter	3	ST15	ST14	ST13	ST12	ST11	ST10	ST9	ST8	00h
Parameter	4	ST7	ST6	ST5	ST4	ST3	ST2	ST1	ST0	40h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below.

Bit	Description	Value
ST31	Booster Voltage Status	"1"=Booster on, "0"=off
ST30	Not Used	"0"
ST29	Not Used	"0"
ST28	Not Used	"0"
ST27	Vertical refresh Order (ML)	"1"=Decrement, "0"=Increment
ST26	RGB/BGR Order (RGB)	"1"=BGR, "0"=RGB
ST25	Horizontal refresh Order (MH)	"1"=Decrement, "0"=Increment
ST24	Not Used	"0"
ST23	Not Used	"0"
ST22-20	Interface Color Pixel Format Definition	"110" = 18-bit / pixel, "111" = 24-bit / pixel
ST19	Idle Mode On/Off	"1" = On, "0" = Off
ST18	Not Used	"0"
ST17	Sleep In/Out	"1" = Out, "0" = In
ST16	Display Normal Mode On/Off	"1" = Normal Display
ST15	Not Used	"0"
ST14	Not Used	"0"
ST13	Inversion Status	"0" = Off
ST12	All Pixels On	"1" = All Pixels On, "0" = All Pixels Off
ST11	All Pixels Off	"0"
ST10	Display On/Off	"1" = On, "0" = Off
ST9	Tearing effect line on/off	"1" = On, "0" = Off
ST8-6	Gamma Curve Selection	"000" = GC0 "001" = GC1 "010" = GC2 "011" = GC3 "100" = GC4 "101" to "111" = Not defined
ST5	Tearing effect line mode	"0" = mode1, "1" = mode2
ST4	Not Used	"0"
ST3	Not Used	"0"
ST2	Not Used	"0"
ST1	Not Used	"0"
ST0	Not Used	"0"

Restriction

-

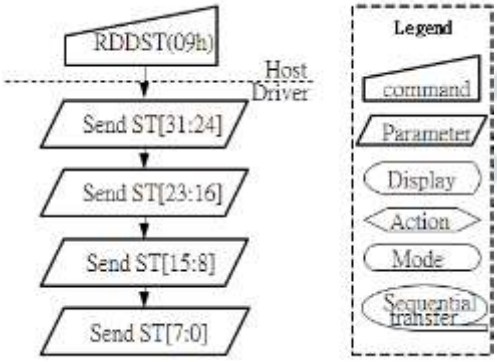
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h,71h,00h,00h
S/W Reset	00h,71h,00h,00h
H/W Reset	00h,71h,00h,00h

Flow Chart



8.2.6 RDDPM: Read Display Power Mode (0Ah)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDPM	R	0	0	0	0	1	0	1	0	0Ah
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	08h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Booster Voltage Status	"1" = Booster on, "0" = Booster off
D6	Idle Mode On/Off	"1" = Idle Mode On, "0" = Idle Mode Off
D5	Not Used	"0"
D4	Sleep In/Out	"1" = Sleep Out, "0" = Sleep In
D3	Display Normal Mode On/Off	"1" = Normal Display On, "0" = Normal Display Off
D2	Display On/Off	"1" = Display On, "0" = Display Off
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

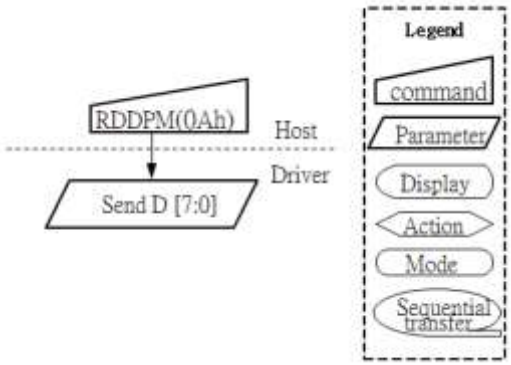
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	08h
S/W Reset	08h
H/W Reset	08h

Flow Chart



8.2.7 RDDMADCTR: Read Display MADCTR (0Bh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDMADCTR	R	0	0	0	0	1	0	1	1	0Bh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Not Used	"0"
D4	Vertical fresh Order (ML)	"1"=Decrement, "0"=Increment
D3	RGB/BGR Order	"1"=BGR, "0"=RGB
D2	Horizontal fresh Order (MH)	"1"=Decrement, "0"=Increment
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

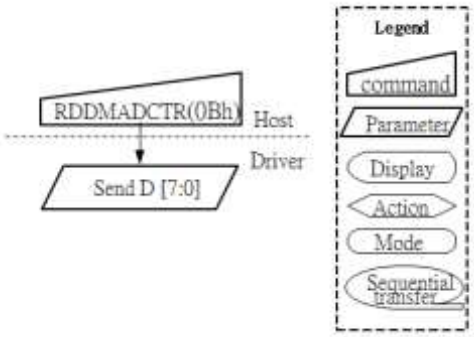
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.8 RDDCOLMOD: Read Display Pixel Format (0Ch)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDCOLMOD	R	0	0	0	0	1	1	0	0	0Ch
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	70h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6 – 4	Control Interface Color Format	"110"=18 bit/pixel "111"=24 bit/pixel The others are not defined
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

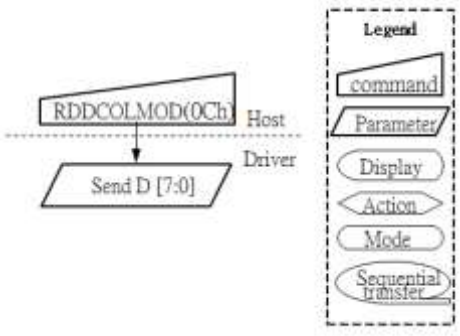
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	70h
H/W Reset	70h

Flow Chart



8.2.9 RDDIM: Read Display Image Mode (0Dh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDIM	R	0	0	0	0	1	1	0	1	0Dh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Not Used	"0"
D6	Not Used	"0"
D5	Inversion On/Off	"0" = Inversion is Off
D4	All Pixels On	"1" = All Pixels On
D3	All Pixels Off	"1" = All Pixels Off
D2 -0	Gamma Curve Selection	"000" = GC1 ,"001" = GC2, "010" = GC3,"011" = GC4 , "100" to "111" are not defined.

Restriction

-

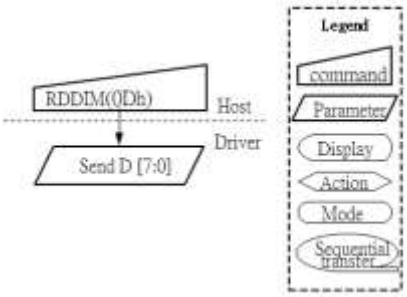
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.10 RDDIM: Read Display Signal Mode (0Eh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSM	R	0	0	0	0	1	1	1	0	0Eh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Tearing Effect Line On/Off	"1" = On, "0" = Off
D6	Tearing effect line mode	"0" = mode1,"1" = mode2
D5	Not Used	"0"
D4	Not Used	"0"
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Error on DSI	"1" = Error, "0" = No Error

Restriction

-

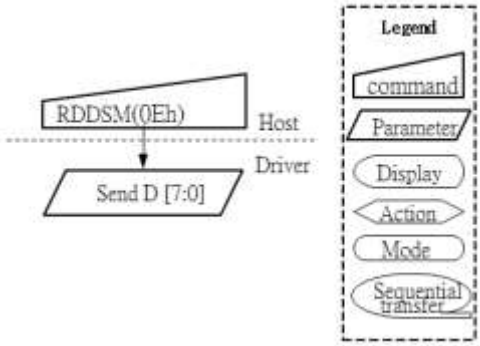
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.11 RDDSDR: Read Display Self-Diagnostic Result (0Fh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDSDR	R	0	0	0	0	1	1	1	1	0Fh
Parameter	1	D7	D6	D5	D4	D3	D2	D1	D0	00h

***NOTE**: "-"Don't care*

Description

This command indicates the current status of the display as described in the table below:

Bit	Description	Value
D7	Register Loading Detection	See Section 6.7.2
D6	Functionality Detection	
D5	Chip Attachment Detection	
D4	Display Glass Break Detection	
D3	Not Used	"0"
D2	Not Used	"0"
D1	Not Used	"0"
D0	Not Used	"0"

Restriction

-

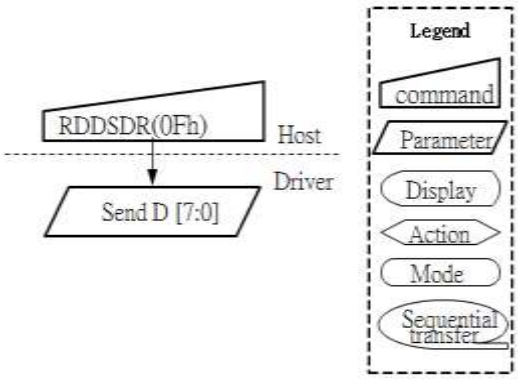
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



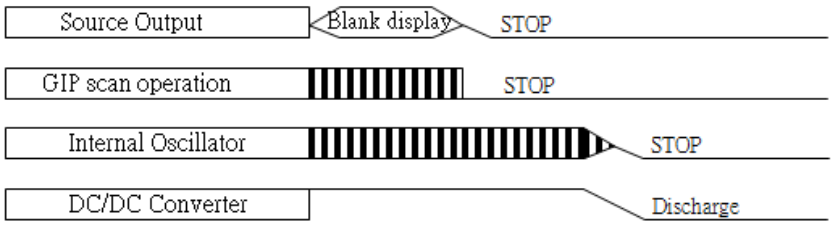
8.2.12 SLPIN: Sleep In (10h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPIN	W	0	0	0	1	0	0	0	0	10h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description

This command causes the LCD module to enter the minimum power consumption mode.
In this mode the DC/DC converter is stopped, Internal display oscillator is stopped, and panel scanning is stopped.



Restriction

This command has no effect when module is already in sleep in mode. Sleep In Mode can only be exit by the Sleep Out Command (11h).
It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize.
It will be necessary to wait 120msec after sending Sleep Out command (when in Sleep In Mode) before Sleep In command can be sent.

Register Availability

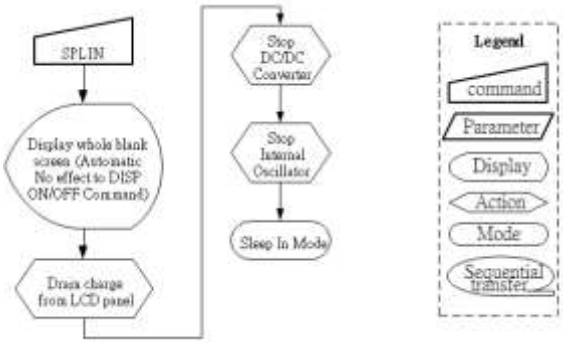
Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Sleep In mode
S/W Reset	Sleep In mode
H/W Reset	Sleep In mode

Flow Chart

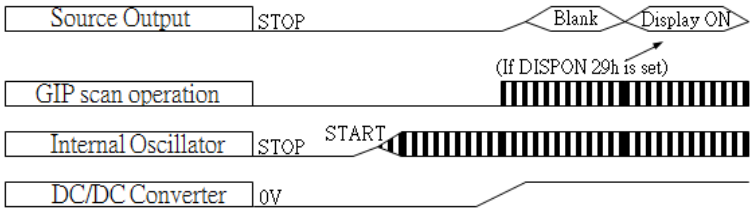
It takes about 120msec to get into Sleep In mode (booster off state) after SLPIN command issued.
The results of booster off can be check by RDDST (09h) command Bit 31.

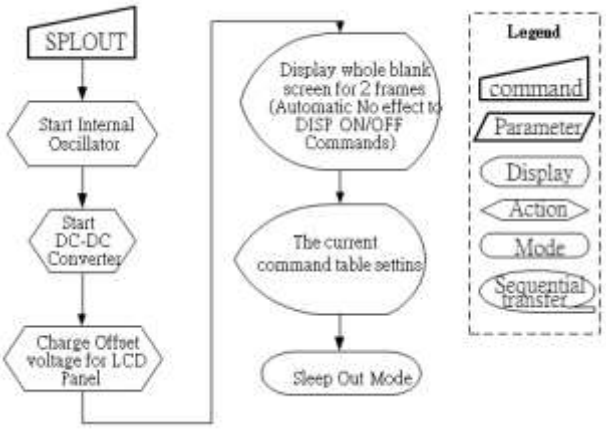


8.2.13 SLPOUT: Sleep Out (11h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
SLPOUT	W	0	0	0	1	0	0	0	1	11h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description	This command turns off sleep mode. In this mode the DC/DC converter is enabled, Internal display oscillator is started, and panel scanning is started. 
Restriction	This command has no effect when module is already in sleep out mode. Sleep Out Mode can only be exit by the Sleep In Command (10h). It will be necessary to wait 5msec before sending next command; this is to allow time for the supply voltages and clock circuits to stabilize. ICNL9707 loads all default values of extended and test command to the registers during this 5msec and there cannot be any abnormal visual effect on the display image if those default and register values are same when this load is done and when the ICNL9707 is already Sleep Out –mode. ICNL9707 is doing self-diagnostic functions during this 5msec. See also section 6.7. It will be necessary to wait 120msec after sending Sleep In command (when in Sleep Out mode) before Sleep Out command can be sent.
Register Availability	<table><tr><th>Status</th><th>Availability</th></tr><tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr><tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr><tr><td>Sleep In</td><td>Yes</td></tr></table>
Default	<table><tr><th>Status</th><th>Default Value</th></tr><tr><td>Power On Sequence</td><td>Sleep In mode</td></tr><tr><td>S/W Reset</td><td>Sleep In mode</td></tr><tr><td>H/W Reset</td><td>Sleep In mode</td></tr></table>

Flow Chart	It takes 120msec to become Sleep Out mode (booster on mode) after SLPOUT command issued. The results of booster on can be checked by RDDST (09h) command Bit 31. 

8.2.14 NORON: Normal Display Mode ON (13h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
NORON	W	0	0	0	1	0	0	1	1	13h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

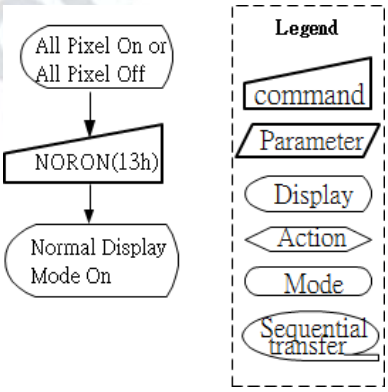
Description	This command returns the display to normal mode. Normal display mode on. Exit from NORON by the All Pixels On or All Pixels Off command. There is no abnormal visual effect during mode change.
Restriction	This command has no effect when Normal Display mode is active.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Normal Mode On
S/W Reset	Normal Mode On
H/W Reset	Normal Mode On

Flow Chart



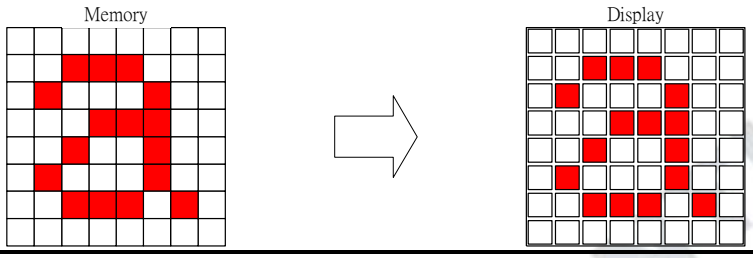
8.2.15 INVOFF: Display Inversion OFF (20h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVOFF	W	0	0	1	0	0	0	0	0	20h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description

This command is used to recover from display inversion mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already inversion off mode.

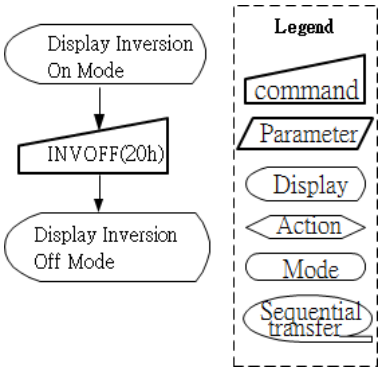
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

Flow Chart



8.2.16 INVON: Display Inversion ON (21h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
INVON	W	0	0	1	0	0	0	0	1	21h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description

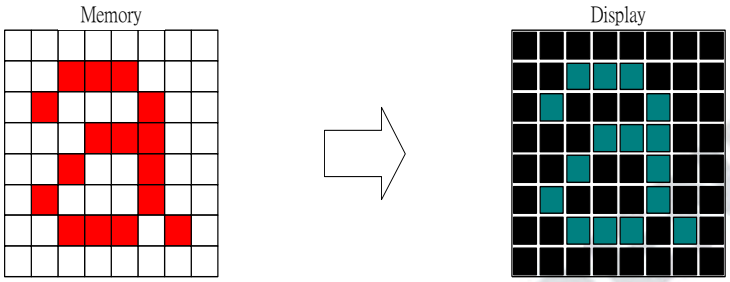
This command is used to enter display inversion mode.

This command makes no change of contents of frame memory.

This command does not change any other status.

To exit from Display Inversion On, the Display Inversion Off command (20h) should be written.

(Example)



Restriction

This command has no effect when module is already inversion On mode.

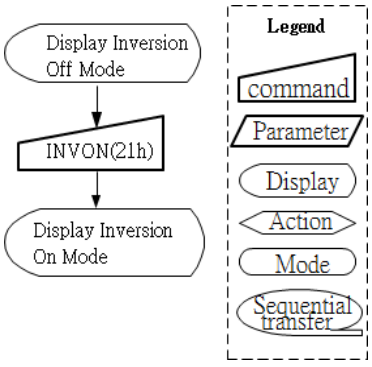
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Inversion Off
S/W Reset	Display Inversion Off
H/W Reset	Display Inversion Off

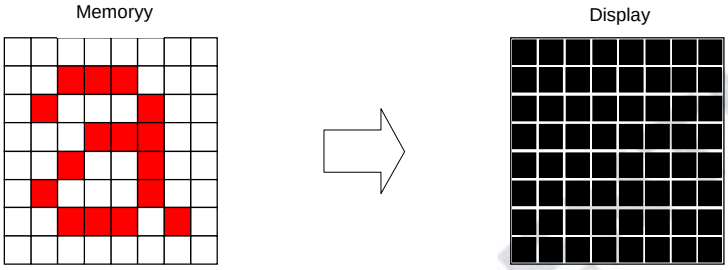
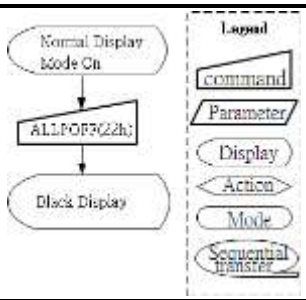
Flow Chart



8.2.17 ALLPOFF: All Pixel OFF (22h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ALLPOFF	W	0	0	1	0	0	0	1	0	22h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description	This command turns the display panel black in Sleep Out mode and a status of the Display On/Off register can be on or off. This command makes no change of contents of frame memory. This command does not change any other status. (Example)  "All Pixels On", "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" command.
Restriction	This command has no effect when module is already in All Pixel Off mode.
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: All Pixels Off Status: S/W Reset — Default Value: All Pixels Off Status: H/W Reset — Default Value: All Pixels Off
Flow Chart	

8.2.18 ALLPON: All Pixel ON (23h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
ALLPON	W	0	0	1	0	0	0	1	1	23h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

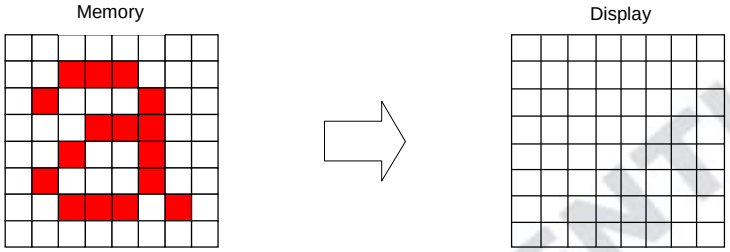
Description

This command turns the display panel white in Sleep Out mode and a status of the Display On/Off register can be on or off.

This command makes no change of contents of frame memory.

This command does not change any other status.

(Example)



"All Pixels OFF", "Normal Display Mode On" commands are used to leave this mode. The display panel is showing the content of the frame memory after "Normal Display On" command.

Restriction

This command has no effect when module is already in All Pixel On mode.

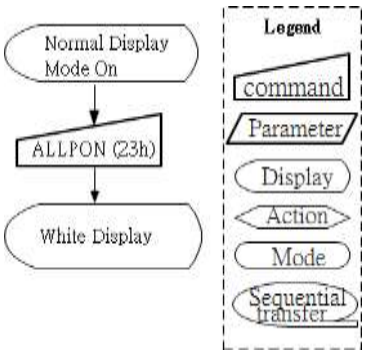
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	All Pixels Off
S/W Reset	All Pixels Off
H/W Reset	All Pixels Off

Flow Chart



8.2.19 GAMSET: Gamma Set (26h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GAMSET	W	0	0	1	0	0	1	1	0	26h
Parameter	1	GC8	GC7	GC6	GC5	GC4	GC3	GC2	GC1	01h

***NOTE**: "-"Don't care*

Description

This command is used to select the desired Gamma curve for the current display. A maximum of 4 curves can be selected. The curve is selected by setting the appropriate bit in the parameter as described in the Table.

GC[7:0]	Parameter	Curve Selected
01h	GC1	Gamma Curve 1 (Gamma=2.2 Set)
02h	GC2	Reserved
04h	GC3	Reserved
08h	GC4	Reserved

***Note**: All other values are undefined.*

Restriction

Values of GC [7:0] not shown in table above are invalid and will not change the current selected gamma curve until valid is received.

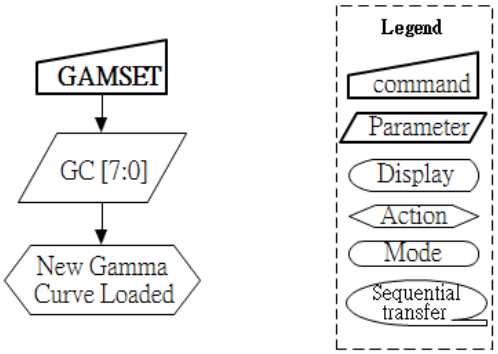
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.20 DISPOFF: Display OFF (28h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPOFF	W	0	0	1	0	1	0	0	0	28h
Parameter	-	No Parameter								

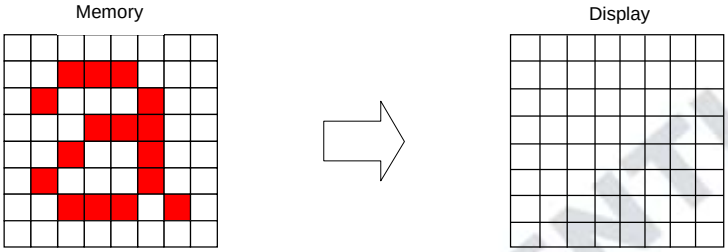
***NOTE**: "-"Don't care*

Description

This command is used to enter into DISPLAY OFF mode. In this mode, the output from Frame Memory is disabled and blank page inserted.

This command makes no change of contents of frame memory. This command does not change any other status. There will be no abnormal visible effect on the display.

(Example)



Restriction

This command has no effect when module is already in Display Off mode.

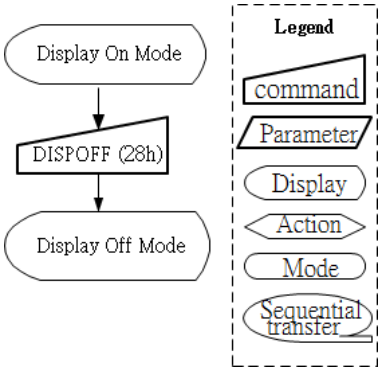
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



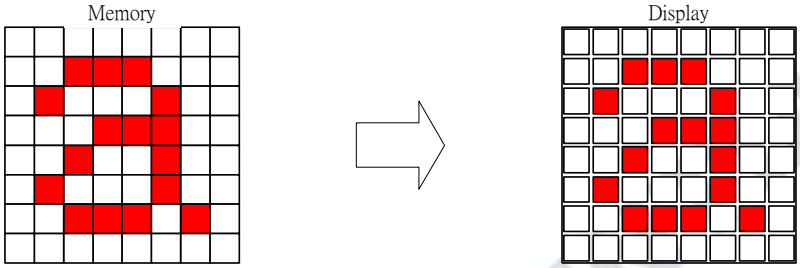
8.2.21 DISPON: Display ON (29h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
DISPON	W	0	0	1	0	1	0	0	1	29h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

Description

This command is used to recover from DISPLAY OFF mode.
This command makes no change of contents of frame memory.
This command does not change any other status.
(Example)



Restriction

This command has no effect when module is already in Display On mode.

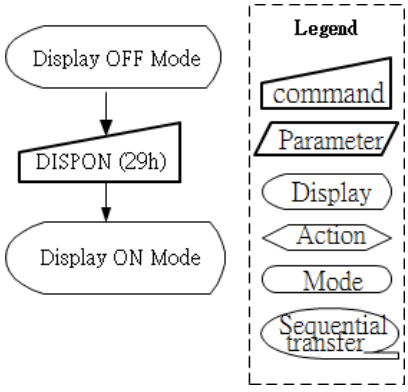
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Display Off
S/W Reset	Display Off
H/W Reset	Display Off

Flow Chart



8.2.22 TEOFF: Tearing Effect Line OFF (34h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEOFF	W	0	0	1	1	0	1	0	0	34h
Parameter	-	No Parameter								

***NOTE**: "-"Don't care*

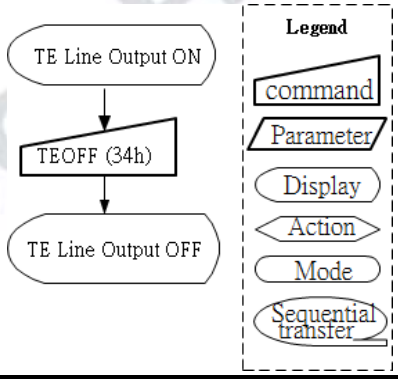
Description	This command is used to turn OFF (Active Low) the Tearing Effect output signal from the TE signal line.
Restriction	This command has no effect when Tearing Effect output is already OFF.
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



8.2.23 TEON: Tearing Effect Line ON (35h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
TEON	W	0	0	1	1	0	1	0	1	35h
Parameter	1	-	-	-	-	-	-	-	M	00h

***NOTE**: "-"Don't care*

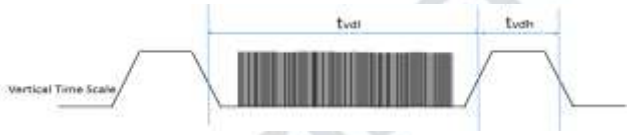
Description

This command is used to turn ON the Tearing Effect output signal from the TE signal line. This output is not affected by changing MADCTL bit ML.

The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line.

When M = "0": The Tearing Effect Output line consists of V-Blanking information only.

When M = "1": The Tearing Effect Output line consists of both V-Blanking and H-Blinking information.



***Note**: During Sleep In Mode with Tearing Effect Line On, Tearing Effect Output pin will be active Low.*

Restriction

This command has no effect when Tearing Effect output is already ON.

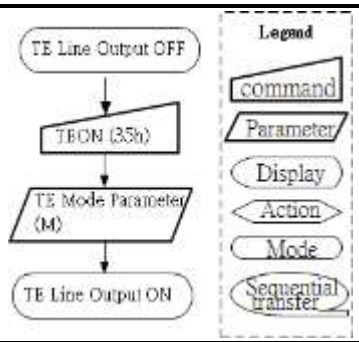
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	Tearing Effect off
S/W Reset	Tearing Effect off
H/W Reset	Tearing Effect off

Flow Chart



8.2.24 MADCTL: Memory Data Access Control (36h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
MADCTL	W	0	0	1	1	0	1	1	0	36h
Parameter	1	-	-	-	ML	RGB	MH	-	-	00h

***NOTE**: "-"Don't care*

Description

This command defines display direction of image.

This command makes no change on the other driver status.

Bit	NAME	DESCRIPTION
ML	Vertical refresh ORDER	LCD Vertical refresh direction control
RGB	RGB-BGR ORDER	Color selector switch control (0=RGB color filter panel, 1=BGR color filter panel)
MH	Horizontal refresh ORDER	LCD Horizontal refresh direction control

Restriction

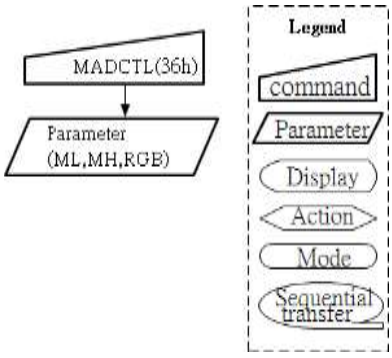
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.25 COLMOD: Interface Pixel Format (3Ah)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
COLMOD	W	0	0	1	1	1	0	1	0	3Ah
Parameter	1	-	VIPF[2:0]			-	-	-	-	70h

***NOTE**: "-"Don't care*

Description

This command is used to define the format of RGB picture data.

The formats are shown in the table:

Bit	NAME	DESCRIPTION
VIPF[2:0]	Pixel Format for RGB.	"110" = 18-bit/pixel "111" = 24-bit/pixel The others = not defined

Restriction

There is no visible effect until the Frame Memory is written to.

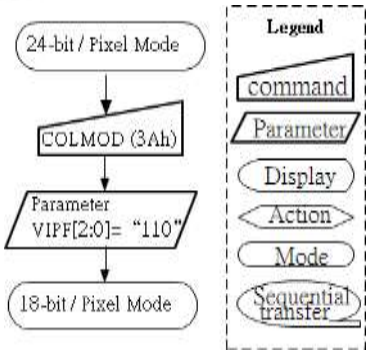
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	70h
S/W Reset	70h
H/W Reset	70h

Flow Chart



8.2.26 STESL: Set Tearing Effect Scan Line (44h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
STESL	W	0	1	0	0	0	1	0	0	44h
Parameter	1	N15	N14	N13	N12	N11	N10	N9	N8	00h
Parameter	1	N7	N6	N5	N4	N3	N2	N1	N0	00h

***NOTE**: "-"Don't care*

Description

This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MADCTL bit ML. The Tearing Effect Line On has one parameter, which describes the mode of the Tearing Effect Output Line mode.
The Tearing Effect Output line consists of V-Blanking information only.

*Note that STESL with N[15:0]="000h" is equivalent to TEON with M="0"*The Tearing Effect Output line shall be active low when the display module is in Sleep in mode.
This command takes effect on the frame following the current frame. Therefore, if the TE output is already on, the TE output shall continue to operate as programmed by the previous "TEON (35h)" or "STESL (44h) command" until the end of the frame.

Restriction

Parameter range 0 _ N[15:0] _ Vactiv+Porch Line

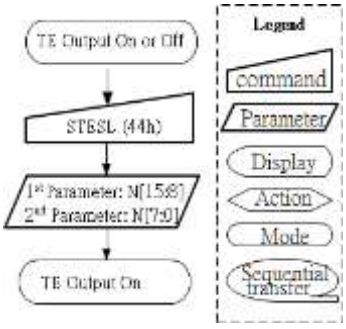
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h

Flow Chart



8.2.27 GSL: Get Scan Line (45h)

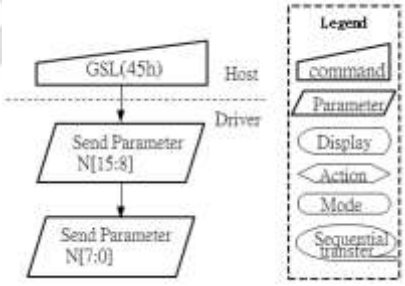
Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
GSL	R	0	1	0	0	0	1	0	1	45h
Parameter	1	N15	N14	N13	N12	N11	N10	N9	N8	00h
Parameter	1	N7	N6	N5	N4	N3	N2	N1	N0	00h

***NOTE**: "-"Don't care*

Description	This command returns the current scan line, N, used to update the display module. The total number of scan lines on display is defined as Vdisplay + Vporch. The first scan line is defined as the first line of V Sync and is denoted as Line 0. When in Sleep in mode, the returned value is undefined.
Restriction	-
Register Availability	
Default	
Flow Chart	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Y,es
Sleep In	Yes

Status	Default Value
Power On Sequence	0000h
S/W Reset	0000h
H/W Reset	0000h



8.2.28 WRDISBV: Write Display Brightness (51h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRDISBV	R	0	1	0	1	0	0	1	0	51h
Parameter	1	BV[15]	BV[14]	BV[13]	BV[12]	BV[11]	BV[10]	BV[9]	BV[8]	00h
Parameter	2	BV[7]	BV[6]	BV[5]	BV[4]	BV[3]	BV[2]	BV[1]	BV[0]	00h

***NOTE**: "-"Don't care*

Description

This command is used to adjust brightness value.

In principle relationship, 51h= 00h 00h value means the lowest brightness, and 51h=0Fh FFh value means the highest brightness.

BV[15:0]	Brightness (Ratio)	Brightness (%)
0000h	0/4096	0%
0001h	1/4096	0.024%
…	…	…
0FFEh	4095/4096	99.97%
0FFFh	4096/4096	100%

Restriction

The display supplier cannot use this command for tuning (e.g. factory tuning, etc.).

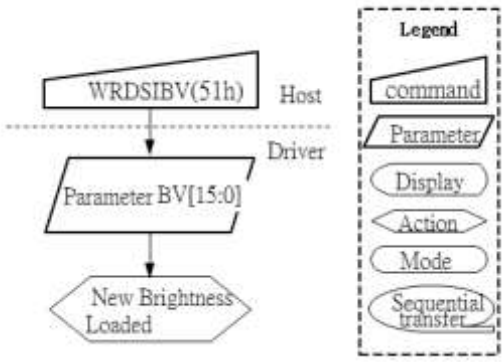
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h 00h
S/W Reset	00h 00h
H/W Reset	00h 00h

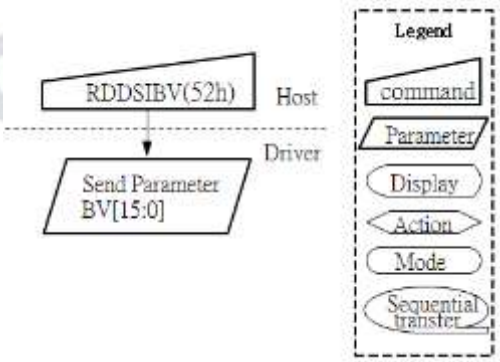
Flow Chart



8.2.29 RDDISBV: Read Display Brightness (52h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDDISBV	R	0	1	0	1	0	0	1	0	52h
Parameter	1	BV[15]	BV[14]	BV[13]	BV[12]	BV[11]	BV[10]	BV[9]	BV[8]	00h
Parameter	2	BV[7]	BV[6]	BV[5]	BV[4]	BV[3]	BV[2]	BV[1]	BV[0]	00h

***NOTE**: "-"Don't care*

<table>
<tr><td>Description</td><td>This command is used to return brightness value.
In principle relationship, 51h= 00h 00h value means the lowest brightness, and 51h=0Fh FFh value means the highest brightness.</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h</td></tr>
<tr><td>S/W Reset</td><td>00h</td></tr>
<tr><td>H/W Reset</td><td>00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

8.2.30 WRCTRLD: Write CTRL Display (53h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCTRLD	W	0	1	0	1	0	0	1	1	53h
Parameter	1	-	-	BCTRL	-	DD	BL	-	-	00h

***NOTE**: "-"Don't care*

Description

This command is used to control display brightness.

BCTRL: Brightness Control Block On/Off. The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit).

BCTRL =0, BV value disable; BCTRL =1, BV value enable.

DD: Display Dimming Control On/Off. DD= 0, Display dimming is off; DD=1, Display dimming is on.

BL: Backlight Control On/Off without Dimming Effect. When BL bit changes from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected. BL =0, Off; BL =1, On.

The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0_1 or 1_0.

Note: All read and write commands are valid, but there is no effect (except registers can be changed) when write commands are used.

Restriction

-

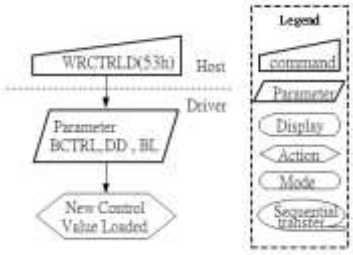
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

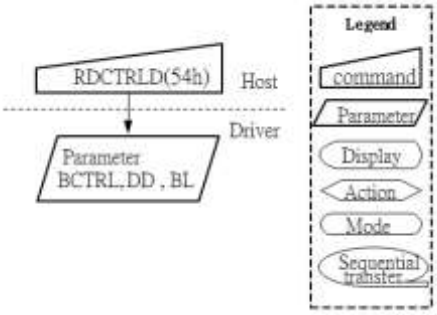
Flow Chart



8.2.31 RDCTRLD: Read CTRL Display (54h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDCTRLD	R	0	1	0	1	0	1	0	0	54h
Parameter	1	-	-	BCTRL	-	DD	BL	-	-	00h

***NOTE**: "-"Don't care*

Description	This command returns the display brightness. BCTRL: Brightness Control Block On/Off The BCTRL bit is always used to switch brightness for display with dimming effect (according to DD bit). BCTRL =0, BV value disable. BCTRL =1, BV value enable. DD: Display Dimming Control On/Off. DD= 0, Display dimming is off. DD=1, Display dimming is on. BL: Backlight Control On/Off without Dimming Effect When BL bit change from "On" to "Off", display brightness is turned off without gradual dimming, even if dimming on (DD="1") is selected. BL =0, Off. BL =1, On The dimming function is adapted to the brightness registers for display when bit BCTRL is changed at DD="1", e.g. BCTRL: 0_1 or 1_0.
Restriction	-
Register Availability	Status: Normal Mode On, Idle Mode Off, Sleep Out — Availability: Yes Status: Normal Mode On, Idle Mode On, Sleep Out — Availability: Yes Status: Sleep In — Availability: Yes
Default	Status: Power On Sequence — Default Value: 00h Status: S/W Reset — Default Value: 00h Status: H/W Reset — Default Value: 00h
Flow Chart	

8.2.32 WRCABC: Write Content Adaptive Brightness Control (55h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCABC	W	0	1	0	1	0	1	0	1	55h
Parameter	1	-	-	-	-	-	-	CABC_CON[1:0]		00h

***NOTE**: "-"Don't care*

Description

This command is used for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC_CON[1:0]		Function
0	0	Off
0	1	User Interface Image
1	0	Still picture
1	1	Moving Image

Restriction

-

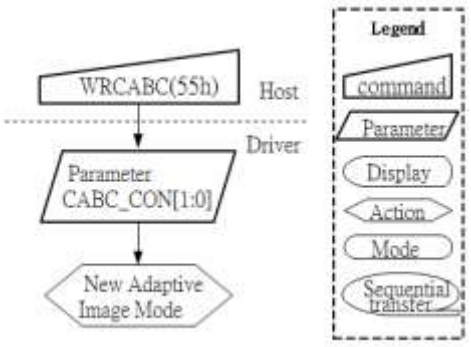
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.33 RDCABC: Read Content Adaptive Brightness Control (56h)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDCABC	R	0	1	0	1	0	1	1	0	56h
Parameter	1	-	-	-	-	-	-	CABC_CON[1:0]		00h

***NOTE**: "-"Don't care*

Description

This command is used to read the settings for image content based adaptive brightness control functionality.

There is possible to use 4 different modes for content adaptive image functionality, which are defined on a table below.

CABC_CON[1:0]		Function
0	0	Off
0	1	User Interface Image
1	0	Still picture
1	1	Moving Image

Restriction

-

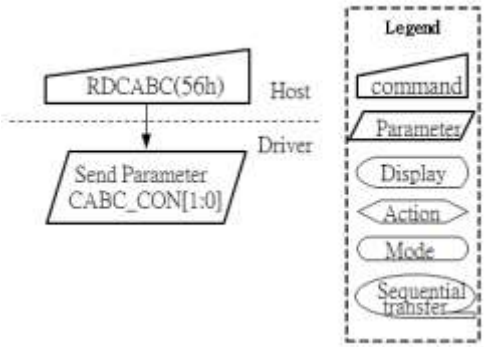
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h
S/W Reset	00h
H/W Reset	00h

Flow Chart



8.2.34 WRCABCMB: Write CABC minimum brightness (5Eh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
WRCABCMB	W	0	1	0	1	1	1	1	0	5Eh
Parameter	1	MB[15]	MB[14]	MB[13]	MB[12]	MB[11]	MB[10]	MB[9]	MB[8]	00h
Parameter	2	MB[7]	MB[6]	MB[5]	MB[4]	MB[3]	MB[2]	MB[1]	MB[0]	00h

***NOTE**: "-"Don't care*

Description

This command is used to set the minimum brightness value of the display for CABC function
In principle relationship, 5Eh= 00h 00h value means the lowest brightness for CABC, and 5Eh = 0Fh FFh value means the highest brightness for CABC.

Restriction

-

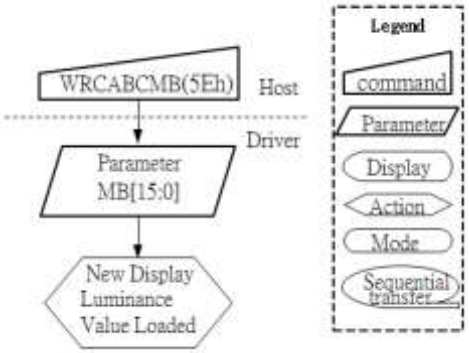
Register Availability

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	00h 00h
S/W Reset	00h 00h
H/W Reset	00h 00h

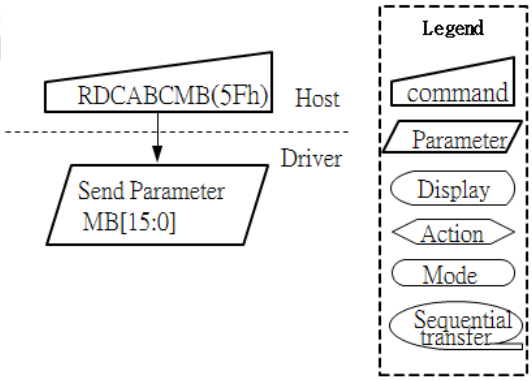
Flow Chart



8.2.35 RDCABCMB: Read CABC minimum brightness (5Fh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDCABCMB	R	0	1	0	1	1	1	1	1	5Fh
Parameter	1	MB[15]	MB[14]	MB[13]	MB[12]	MB[11]	MB[10]	MB[9]	MB[8]	00h
Parameter	2	MB[7]	MB[6]	MB[5]	MB[4]	MB[3]	MB[2]	MB[1]	MB[0]	00h

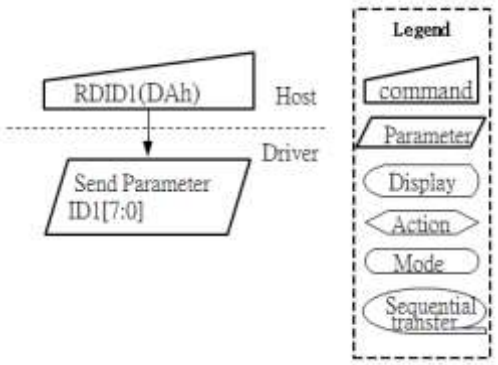
***NOTE**: "-"Don't care*

<table>
<tr><td>Description</td><td>This command return the minimum brightness value of CABC function. In principle relationship is that 0000h value means the lowest brightness for CABC and FFh value means the highest brightness for CABC. MB[15:0] is the minimum brightness for CABC specified with "WRCABCMB Write CABC minimum brightness (5Eh)" command.</td></tr>
<tr><td>Restriction</td><td>-</td></tr>
<tr><td>Register Availability</td><td>
<table>
<tr><th>Status</th><th>Availability</th></tr>
<tr><td>Normal Mode On, Idle Mode Off, Sleep Out</td><td>Yes</td></tr>
<tr><td>Normal Mode On, Idle Mode On, Sleep Out</td><td>Yes</td></tr>
<tr><td>Sleep In</td><td>Yes</td></tr>
</table>
</td></tr>
<tr><td>Default</td><td>
<table>
<tr><th>Status</th><th>Default Value</th></tr>
<tr><td>Power On Sequence</td><td>00h 00h</td></tr>
<tr><td>S/W Reset</td><td>00h 00h</td></tr>
<tr><td>H/W Reset</td><td>00h 00h</td></tr>
</table>
</td></tr>
<tr><td>Flow Chart</td><td> 
</td></tr>
</table>

8.2.36 RDID1: Read ID1 Value (DAh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID1	R	1	1	0	1	1	0	1	0	DAh
Parameter	1	ID1[7]	ID1[6]	ID1[5]	ID1[4]	ID1[3]	ID1[2]	ID1[1]	ID1[0]	FFh

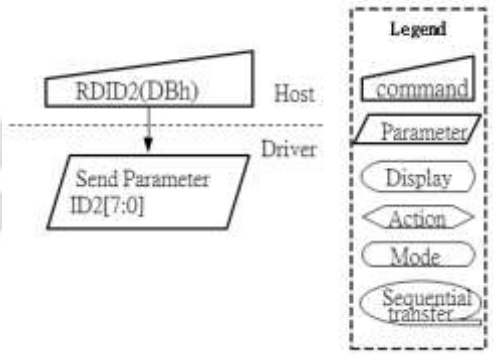
***NOTE**: "-"Don't care*

Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / FFh S/W Reset / FFh H/W Reset / FFh
Flow Chart	

8.2.37 RDID2: Read ID2 Value (DBh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID2	R	1	1	0	1	1	0	1	1	DBh
Parameter	1	ID2[7]	ID2[6]	ID2[5]	ID2[4]	ID2[3]	ID2[2]	ID2[1]	ID2[0]	FFh

***NOTE**: "-"Don't care*

Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-
Register Availability	Status / Availability Normal Mode On, Idle Mode Off, Sleep Out / Yes Normal Mode On, Idle Mode On, Sleep Out / Yes Sleep In / Yes
Default	Status / Default Value Power On Sequence / FFh S/W Reset / FFh H/W Reset / FFh
Flow Chart	

8.2.38 RDID3: Read ID3 Value (DCh)

Inst / Para	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Hex
RDID3	R	1	1	0	1	1	1	0	0	DCh
Parameter	1	ID3[7]	ID3[6]	ID3[5]	ID3[4]	ID3[3]	ID3[2]	ID3[1]	ID3[0]	FFh

***NOTE**: "-"Don't care*

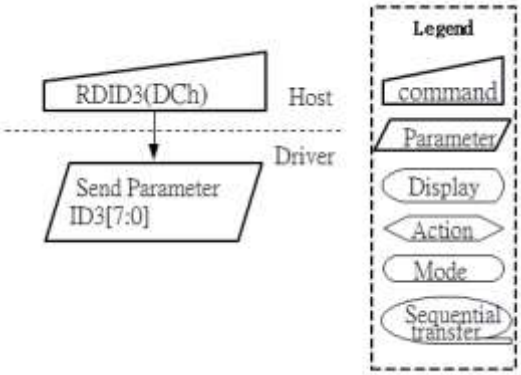
Description	This read byte identifies the TFT LCD module's manufacture ID.
Restriction	-
Register Availability	

Status	Availability
Normal Mode On, Idle Mode Off, Sleep Out	Yes
Normal Mode On, Idle Mode On, Sleep Out	Yes
Sleep In	Yes

Default

Status	Default Value
Power On Sequence	FFh
S/W Reset	FFh
H/W Reset	FFh

Flow Chart



8.3 Command 2 Description

8.3.1 CGout_L Control

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
Gout_L		1	0	1	1	0	0	1	1	B3h
Parameter	1	0	0	GOUTL_SEL 1 [5:0]						03h
	2	0	0	GOUTL_SEL 2 [5:0]						03h
	3	0	0	GOUTL_SEL 3 [5:0]						03h
	4	0	0	GOUTL_SEL 4 [5:0]						03h
	5	0	0	GOUTL_SEL 5 [5:0]						03h
	6	0	0	GOUTL_SEL 6 [5:0]						03h
	7	0	0	GOUTL_SEL 7 [5:0]						03h
	8	0	0	GOUTL_SEL 8 [5:0]						03h
	9	0	0	GOUTL_SEL 9 [5:0]						03h
	10	0	0	GOUTL_SEL 10 [5:0]						03h
	11	0	0	GOUTL_SEL 11 [5:0]						03h
	12	0	0	GOUTL_SEL 12 [5:0]						03h
	13	0	0	GOUTL_SEL 13 [5:0]						03h
	14	0	0	GOUTL_SEL 14 [5:0]						03h
	15	0	0	GOUTL_SEL 15 [5:0]						03h
	16	0	0	GOUTL_SEL 16 [5:0]						03h
	17	0	0	GOUTL_SEL 17 [5:0]						03h
	18	0	0	GOUTL_SEL 18 [5:0]						03h
	19	0	0	GOUTL_SEL 19 [5:0]						03h
	20	0	0	GOUTL_SEL 20 [5:0]						03h
	21	0	0	GOUTL_SEL 21 [5:0]						03h
	22	0	0	GOUTL_SEL 22 [5:0]						03h

H/W reset Default value

Parameter	Value
GOUTL_SEL_1~22[5:0]	03h

Description

Set the mapping of the left-side ASG signals.

Function

Hex	Output signal	Remark
00h	VGL	
01h	VGH	
02h	Hi-Z	
03h	GND	
04h	GSP1	
05h	GSP2	
06h	GSP3	
07h	GSP4	
08h	GCK1	
09h	GCK2	
0Ah	GCK3	
0Bh	GCK4	
0Ch	GCK5	
0Dh	GCK6	
0Eh	GCK7	

		0Fh	GCK8		
		10h	GCK9	Option for BI1	
		11h	GCK10	Option for BI2	
		12h	GCK11	Option for BI3	
		13h	GCK12	Option for BI4	
		14h	GCK13	Option for BI5	
		15h	GCK14	Option for BI6	
		16h	GCK15	Option for BI7	
		17h	GCK16	Option for BI8	
		18h	DIR	Scan direction setting	
		19h	DIRB	Scan direction setting	
		1Ah	ECLK_AC	Frame toggle signal	
		1Bh	ECLK_ACB	Frame toggle signal	
		1Ch	ECLK_AC2	Frame toggle signal	
		1Dh	ECLK_ACB2		
		1Eh	GCH		
		1Fh	GCL		
		20h	XDON		
		21h	XDONB		
		22h	GOA_RESET		
		23h	GCK1		
		24h	GCK2		
		25h	GCK3		
		26h	GCK4		
		27h~3Fh	(Reserved)		

8.3.2 CCGout_R Control

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
Gout_L		1	0	1	1	0	1	0	0	B4h
Parameter	1	0	0	GOUTR_SEL 1 [5:0]						03h
	2	0	0	GOUTR_SEL 2 [5:0]						03h
	3	0	0	GOUTR_SEL 3 [5:0]						03h
	4	0	0	GOUTR_SEL 4 [5:0]						03h
	5	0	0	GOUTR_SEL 5 [5:0]						03h
	6	0	0	GOUTR_SEL 6 [5:0]						03h
	7	0	0	GOUTR_SEL 7 [5:0]						03h
	8	0	0	GOUTR_SEL 8 [5:0]						03h
	9	0	0	GOUTR_SEL 9 [5:0]						03h
	10	0	0	GOUTR_SEL 10 [5:0]						03h
	11	0	0	GOUTR_SEL 11 [5:0]						03h
	12	0	0	GOUTR_SEL 12 [5:0]						03h
	13	0	0	GOUTR_SEL 13 [5:0]						03h
	14	0	0	GOUTR_SEL 14 [5:0]						03h
	15	0	0	GOUTR_SEL 15 [5:0]						03h
	16	0	0	GOUTR_SEL 16 [5:0]						03h
	17	0	0	GOUTR_SEL 17 [5:0]						03h
	18	0	0	GOUTR_SEL 18 [5:0]						03h
	19	0	0	GOUTR_SEL 19 [5:0]						03h
	20	0	0	GOUTR_SEL 20 [5:0]						03h
	21	0	0	GOUTR_SEL 21 [5:0]						03h
	22	0	0	GOUTR_SEL 22 [5:0]						03h

H/W reset Default value

Parameter	Value
GOUTR_SEL_1~22[5:0]	03h

Description

Set the mapping of the right-side ASG signals.

Function

Hex	Output signal	Remark
00h	VGL	
01h	VGH	
02h	Hi-Z	
03h	GND	
04h	GSP1	
05h	GSP2	
06h	GSP3	
07h	GSP4	
08h	GCK1	
09h	GCK2	
0Ah	GCK3	
0Bh	GCK4	
0Ch	GCK5	
0Dh	GCK6	
0Eh	GCK7	
0Fh	GCK8	
10h	GCK9	Option for BI1
11h	GCK10	Option for BI2

		12h	GCK11	Option for BI3	
		13h	GCK12	Option for BI4	
		14h	GCK13	Option for BI5	
		15h	GCK14	Option for BI6	
		16h	GCK15	Option for BI7	
		17h	GCK16	Option for BI8	
		18h	DIR	Scan direction setting	
		19h	DIRB	Scan direction setting	
		1Ah	ECLK_AC	Frame toggle signal	
		1Bh	ECLK_ACB	Frame toggle signal	
		1Ch	ECLK_AC2	Frame toggle signal	
		1Dh	ECLK_ACB2		
		1Eh	GCH		
		1Fh	GCL		
		20h	XDON		
		21h	XDONB		
		22h	GOA_RESET		
		23h	GCK1		
		24h	GCK2		
		25h	GCK3		
		26h	GCK4		
		27h~3Fh	(Reserved)		

8.3.3 SETID

<table>
<tr><th colspan="2">Inst / Para</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td colspan="2">SETID</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>B5h</td></tr>
<tr><td rowspan="4">Parameter</td><td>1</td><td colspan="8">ID1[7:0]</td><td>FFh</td></tr>
<tr><td>2</td><td colspan="8">ID2[7:0]</td><td>FFh</td></tr>
<tr><td>3</td><td colspan="8">ID3[7:0]</td><td>FFh</td></tr>
<tr><td>4</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td colspan="3">OTP_ID_TIMES[2:0]</td><td>00h</td></tr>
<tr><td>H/W reset Default value</td><td colspan="10"><table><tr><th>Parameter</th><th>Value</th></tr><tr><td>ID1[7:0]</td><td>FFh</td></tr><tr><td>ID2[7:0]</td><td>FFh</td></tr><tr><td>ID3[7:0]</td><td>FFh</td></tr><tr><td>OTP_ID_TIMES[2:0]</td><td>00h</td></tr></table></td></tr>
<tr><td rowspan="4">Description</td><td colspan="2">ID1[7:0]</td><td colspan="8" rowspan="3">Set ID1, ID2, ID3 value.</td></tr>
<tr><td colspan="2">ID2[7:0]</td></tr>
<tr><td colspan="2">ID3[7:0]</td></tr>
<tr><td colspan="2">OTP_ID_TIMES[2:0]</td><td colspan="8">OTP_TIMES [2:0] show the remaining program times status.</td></tr>
<tr><td>Function</td><td colspan="10">Description as above.</td></tr>
</table>

8.3.4 PWRCON_VCOM

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_VCOM		1	0	1	1	0	1	1	0	B6h
Parameter	1	VCOM_FWS[7:0]								2Fh
	2	VCOM_BWS[7:0]								2Fh
	3	0	0	0	0	0	OTP_VCOM_TIMES[2:0]			00h

H/W reset Default value

Parameter	Value
VCOM_FWS[7:0]	2Fh
VCOM_BWS[7:0]	2Fh
OTP_VCOM_TIMES[2:0]	00h

VCOM_FWS[7:0]	This register set forward scan VCOM voltage. Register Step 15mV
VCOM_BWS[7:0]	This register set backward scan VCOM voltage. Register Step 15mV
OTP_VCOM_TIMES[2:0]	OTP_VCOM_TIMES[2:0] show the VCOM program times status.

Function

VCOM_FWS[7:0], VCOM_BWS[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	VCOM(V)
0	0	0	0	0	0	0	0	00h	-0.3
0	0	0	0	0	0	0	1	01h	-0.315
0	0	0	0	0	0	1	0	02h	-0.33
0	0	0	0	0	0	1	1	03h	-0.345
0	0	0	0	0	1	0	0	04h	-0.36
0	0	0	0	0	1	0	1	05h	-0.375
0	0	0	0	0	1	1	0	06h	-0.39
…	…	…	…	…	…	…	…	…	…
0	0	1	1	1	1	0	0	3Ch	-1.2
0	0	1	1	1	1	0	1	3Dh	-1.215
0	0	1	1	1	1	1	0	3Eh	-1.23
0	0	1	1	1	1	1	1	3Fh	-1.245
…	…	…	…	…	…	…	…	…	…
1	1	1	1	0	1	1	1	F7h	-4.005
1	1	1	1	1	0	0	0	F8h	Inhibited
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	FFh	Inhibited

8.3.5 PWRCON_SEQ

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_SEQ		1	0	1	1	0	1	1	1	B7h
Parameter	1	0	0	VSP_DC_H[5:0]						01h
	2	0	0	VSN_DC_H[5:0]						01h
	3	0	0	VCL_DC_H[5:0]						09h
	4	0	0	VGH_DC_H[5:0]						0Dh
	5	0	0	VGL_DC_H[5:0]						11h
	6	0	0	GAM_DC_H[5:0]						19h
	7	0	0	VCOM_DC_H[5:0]						1Dh
	8	0	0	RT_DC_H[5:0]						15h
	9	0	0	0	0	0	0	0	0	00h
	10	0	0	GATE_ON_DC_H[5:0]						25h
	11	0	0	SOFT_L[5:0]						32h
	12	VCL_DC_L[3:0]				VSP_DC_L[3:0]				00h
	13	VCOM_DC_L[3:0]				VGL_DC_L[3:0]				00h
	14	VGH_DC_L[3:0]				VSN_DC_L[3:0]				00h
	15	RT_DC_L[3:0]				GAM_DC_L[3:0]				00h
	16	GATE_ON_DC_L[3:0]				DISCH_L[3:0]				02h
	17	1	1	1	1	0	1	1	1	F7h
	18	0	0	1	1	1	0	0	0	38h

H/W reset Default value

Parameter	Value
VSP_DC_H[5:0]	01h
VSN_DC_H[5:0]	01h
VCL_DC_H[5:0]	09h
VGH_DC_H[5:0]	0Dh
VGL_DC_H[5:0]	11h
GAM_DC_H[5:0]	19h
VCOM_DC_H[5:0]	1Dh
RT_DC_H[5:0]	15h
GATE_ON_DC_H[5:0]	25h
SOFT_L[5:0]	32h
VCL_DC_L[3:0]	00h
VCOM_DC_L[3:0]	00h
VGH_DC_L[3:0]	00h
RT_DC_L[3:0]	00h
GATE_ON_DC_L[3:0]	00h
VSP_DC_L[3:0]	00h
VGL_DC_L[3:0]	00h
VSN_DC_L[3:0]	00h

		GAM_DC_L[3:0]	00h
		DISCH_L[3:0]	02h
Description	VSP_DC_H[5:0]	VSP enable sequence. Register step is 2ms.	
	VSN_DC_H[5:0]	VSN enable sequence. Register step is 2ms.	
	VCL_DC_H[5:0]	VCL enable sequence. Register step is 2ms.	
	VGH_DC_H[5:0]	VGH enable sequence. Register step is 2ms.	
	VGL_DC_H[5:0]	VGL enable sequence. Register step is 2ms.	
	GAM_DC_H[5:0]	VGAM enable sequence. Register step is 2ms.	
	VCOM_DC_H[5:0]	VCOM enable sequence. Register step is 2ms.	
	RT_DC_H[5:0]	RT enable sequence. Register step is 2ms.	
	GATE_ON_DC_H[5:0]	Gate on enable sequence. Register step is 2ms.	
	SOFT_L[5:0]	Soft enable sequence. Register step is 2ms.	
	VCL_DC_L[3:0]	VCL enable sequence. Register step is 2ms.	
	VCOM_DC_L[3:0]	VCOM disable sequence. Register step is 2ms.	
	VGH_DC_L[3:0]	VGH disable sequence. Register step is 2ms.	
	RT_DC_L[3:0]	VRT disable sequence. Register step is 2ms.	
	GATE_ON_DC_L[3:0]	GATE disable sequence. Register step is 2ms.	
	VSP_DC_L[3:0]	VSP disable sequence. Register step is 2ms.	
	VGL_DC_L[3:0]	VGL disable sequence. Register step is 2ms.	
	VSN_DC_L[3:0]	VSN disable sequence. Register step is 2ms.	
	GAM_DC_L[3:0]	VGM disable sequence. Register step is 2ms.	
	DISCH_L[3:0]	Enable discharge circuit sequence. Register step is 2ms.	

Function

XXX_DC_H[5:0] 、 XXX_DC_L[3:0]									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**	**Time(ms)**
0	0	0	0	0	0	0	0	00h	0
0	0	0	0	0	0	0	1	01h	2
0	0	0	0	0	0	1	0	02h	4
0	0	0	0	0	0	1	1	03h	6
…	…	…	…	…	…	…	…	…	…
0	0	1	1	1	1	0	1	3dh	124
0	0	1	1	1	1	1	0	3Eh	124
0	0	1	1	1	1	1	1	3Fh	126

8.3.6 PWRCON_CLK

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_CLK		1	0	1	1	1	0	0	0	B8h
Parameter	1	VCOM_EN_S[1:0]		1	1	DCDC_RT[1:0]		OTP_DCDC_RT[1:0]		34
	2	0	PWRIC_CLK_S[2:0]			0	0	1	1	53
	3	0	0	0	0	DCDC_CLK_NS[3:0]				03
	4	1	1	0	0	1	1	0	0	CC

H/W reset Default value

Parameter	Value
VCOM_EN_S[1:0]	00h
DCDC_RT[1:0]	01h
OTP_DCDC_RT[1:0]	00h
PWRIC_CLK_S[2:0]	05h
DCDC_CLK_SS[3:0]	03h
DCDC_CLK_NS[3:0]	03h

Description

VCOM_EN_S[1:0]	Set VCOM Output
DCDC_RT[1:0]	Set VGH and VGL charge pump circuit
OTP_DCDC_RT[1:0]	Set OTP programming power charge pump circuit
PWRIC_CLK_S[2:0]	Set VCSW1 and VCSW 2 output clock.
DCDC_CLK_NS[3:0]	Set VGH and VGL charge pump clock

Function

VCOM_EN_S[1:0]			
D1	D0	HEX	VCOM output
0	0	00h	Follow VCOM_DC_H[5:0]
0	1	01h	Sleep out command
1	0	02h	Display on command
1	1	03h	Inhibited

DCDC_RT[1:0]				
D1	D0	HEX	VGH pump ratio	VGL pump ratio
0	0	00h	2*VSP-VSN	VSN-VSP
0	1	01h	2*VSP-VSN	2*VSN-VSP
1	0	02h	3*VSP-VSN	VSN-2*VSP
1	1	03h	3*VSP-VSN	2*VSN-2*VSP

OTP_DCDC_RT[1:0]			
D1	D0	HEX	OTP_VGH pump ratio
0	0	00h	2*VSP-VSN
0	1	01h	2*VSP-VSN
1	0	02h	3*VSP-VSN
1	1	03h	3*VSP-VSN

PWRIC_CLK_S[2:0]				
D2	D1	D0	HEX	CLK period
0	0	0	00h	1/8 HS
0	0	1	01h	1/4 HS
0	1	0	02h	1/2 HS
0	1	1	03h	1 HS
1	0	0	04h	2 HS
1	0	1	05h	4 HS
1	1	0	06h	6 HS
1	1	1	07h	8 HS

DCDC_CLK_NS[3:0]					
D3	D2	D1	D0	HEX	CLK period
0	0	0	0	00h	1/4HS
0	0	0	1	01h	1/2HS
0	0	1	0	02h	HS
0	0	1	1	03h	2HS
0	1	0	0	04h	4HS
0	1	0	1	05h	8HS
0	1	1	0	06h	(Reserved)
0	1	1	1	07h	(Reserved)
1	0	0	0	08h	(Reserved)
...	...	...	...	...	...
1	1	1	1	0Fh	(Reserved)

8.3.7 PWRCON_BTA

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_BTA		1	0	1	1	1	0	0	1	B9h
Parameter	1	1	0	1	0	0	GAS_VSP_EN	0	1	A5
	2	0	0	1	0	0	0	0	0	20
	3	1	1	1	1	1	1	1	1	FF
	4	GAS_IO_EN	GAS_IO_S[2:0]			GAS_VSP_S[3:0]				CA

H/W reset Default value

Parameter	Value
GAS_IO_EN	01h
GAS_VSP_EN	01h
GAS_IO_S[2:0]	04h
GAS_VSP_S[3:0]	0AH

Description

GAS_IO_EN	Set IOVCC abnormal off detection function.
GAS_VSP_EN	Set VSP abnormal off detection function.
GAS_IO_S[2:0]	Set IOVCC detect value.
GAS_VSP_S[3:0]	Set VSP detect value.

Function

GAS_IO_S[2:0]				
D2	D1	D0	HEX	IOVCC (V)
0	0	0	00h	0.9
0	0	1	01h	1
0	1	0	02h	1.1
0	1	1	03h	1.2
1	0	0	04h	1.3
1	0	1	05h	1.4
1	1	0	06h	1.5
1	1	1	07h	1.6

GAS_VSP_S[2:0]					
D3	D2	D1	D0	HEX	VSP (V)
0	0	0	0	00h	2.83
				01h	2.90
0	0	1	0	02h	2.98
0	0	1	1	03h	3.06
0	1	0	0	04h	3.14
0	1	0	1	05h	3.23
0	1	1	0	06h	3.32
0	1	1	1	07h	3.42
1	0	0	0	08h	3.53
1	0	0	1	09h	3.64

		1	0	1	0	0Ah	3.76
		1	0	1	1	0Bh	3.89
		1	1	0	0	0Ch	4.03
		1	1	0	1	0Dh	4.17
		1	1	1	0	0Eh	4.33
		1	1	1	1	0Fh	4.5

8.3.8 PWRCON_MODE

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_MODE		1	0	1	1	1	0	1	0	BAh
Parameter	1	VCSW2_HZ	VCSW2_S[2:0]			VCSW1_HZ	VCSW1_S[2:0]			27h
	2	POWERIC_CLK_EN	0	1	1	0	0	1	1	33h

H/W reset Default value

Parameter	Value
VCSW2_HZ	00h
VCSW2_S[2:0]	02h
VCSW1_HZ	00h
VCSW1_S[2:0]	07h
POWERIC_CLK_EN	00h

Description

VCSW2_HZ	Set VCSW2 Floating.
VCSW2_S[2:0]	Set VCSW2 output status.
VCSW1_HZ	Set VCSW1 Floating.
VCSW1_S[2:0]	Set VCSW1 output status.
POWERIC_CLK_EN	Enable PWRIC_CLK when PMIC mode application

Function

VCSW1_S[2:0] , VCSW2_S[2:0]				
D2	D1	D0	HEX	Output signal
0	0	0	00h	VCI
0	0	1	01h	GND
0	1	0	02h	PWRIC_CLK
0	1	1	03h	Inhibited
1	0	0	04h	Inhibited
1	0	i	05h	Inhibited
1	1	0	06h	Inhibited
1	1	1	07h	VSP_DC

8.3.9 PWRCON_REG

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_REG		1	0	1	1	1	1	0	1	BDh
Parameter	1	VDDN_VCOM_S[2:0]			0	0	0	1	1	43
	2	0	0	0	0	1	1	1	0	0E
	3	0	0	0	0	1	1	1	0	0E
	4	VGMP_S[7:0]								4B
	5	VGMN_S[7:0]								4B
	6	0	0	VGH_S[5:0]						14
	7	0	0	VGL_S[5:0]						14
	8	0	0	OTP_VGH_S[5:0]						03
	9	0	VDDDL_S[2:0]			0	VDDDR_S[2:0]			44
	10	0	0	0	0	0	VDDD_SLPIN_S[2:0]			03

H/W reset Default value

Parameter	Value
VDDN_VCOM_S[2:0]	01h
VGMP_S[7:0]	4Bh
VGMN_S[7:0]	4Bh
VGH_S[5:0]	14h
VGL_S[5:0]	14h
OTP_VGH_S[5:0]	03h

Description

VDDN_VCOM_S[2:0]	Set VDDN_VCOM output voltage, for VCL pad output. Register step is 300mV.
VGMP_S[7:0]	Set VGMP output voltage for Positive Gamma. Register step is 20mV.
VGMN_S[7:0]	Set VGMN output voltage for Positive Gamma. Register step is 20mV.
VGH_S[5:0]	Set VGH output voltage. Register step is 200mV.
VGL_S[5:0]	Set VGL output voltage. Register step is 200mV.
OTP_VGH_S[5:0]	Set VGH power for OTP cell. Register step is 200mV.

Function

VDDN_VCOM_S[2:0]				
D2	D1	D0	HEX	Values (V)
0	0	0	0h	-2.5
0	0	1	1h	-2.8
0	1	0	2h	-3.1
0	1	1	3h	-3.4
1	0	0	4h	-3.7
1	0	1	5h	-4
1	1	0	6h	-4.3
1	1	1	7h	-4.6

VGMP_S[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	VGMP(V)
0	0	0	0	0	0	0	0	00h	3
0	0	0	0	0	0	0	1	01h	3.02
0	0	0	0	0	0	1	0	02h	3.04
0	0	0	0	0	0	1	1	03h	3.06
0	0	0	0	0	1	0	0	04h	3.08
…	…	…	…	…	…	…	…	…	…
0	1	0	0	1	0	1	0	4Ah	4.48
0	1	0	0	1	0	1	1	4Bh	4.5
0	1	0	0	1	1	0	0	4Ch	4.52
…	…	…	…	…	…	…	…	…	…
1	0	0	1	0	1	0	0	94h	5.96
1	0	0	1	0	1	0	1	95h	5.98
1	0	0	1	0	1	1	0	96h	6
1	0	0	1	0	1	1	1	97h	Inhibited
…	…	…	…	…	…	…	…	…	Inhibited
1	1	1	1	1	1	1	1	FFh	Inhibited

VGMN_S[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	VGMP(V)
0	0	0	0	0	0	0	0	00h	-3
0	0	0	0	0	0	0	1	01h	-3.02
0	0	0	0	0	0	1	0	02h	-3.04
0	0	0	0	0	0	1	1	03h	-3.06
0	0	0	0	0	1	0	0	04h	-3.08
…	…	…	…	…	…	…	…	…	……
0	1	0	0	1	0	1	0	4Ah	-4.48
0	1	0	0	1	0	1	1	4Bh	-4.5
0	1	0	0	1	1	0	0	4Ch	-4.52
…	…	…	…	…	…	…	…	…	…
1	0	0	1	0	1	0	0	94h	-5.96
1	0	0	1	0	1	0	1	95h	-5.98
1	0	0	1	0	1	1	0	96h	-6
1	0	0	1	0	1	1	1	97h	Inhibited
…	…	…	…	…	…	…	…	…	Inhibited
1	1	1	1	1	1	1	1	FFh	Inhibited

VGH_S [5:0] , OTP_VGH_S[5:0]							
D5	D4	D3	D2	D1	D0	HEX	Value (V)
0	0	0	0	0	0	00h	8.6
0	0	0	0	0	1	01h	8.8
0	0	0	0	1	0	02h	9
0	0	0	0	1	1	03h	9.2
0	0	0	1	0	0	04h	9.4
…	…	…	…	…	…	…	…
0	1	0	0	1	0	12h	12.2
0	1	0	0	1	1	13h	12.4
0	1	0	1	0	0	14h	12.6
0	1	0	1	0	1	15h	12.8
0	1	0	1	1	0	16h	13
…	…	…	…	…	…	…	…
1	1	1	0	1	1	FBh	20.4
1	1	1	1	0	0	FCh	20.6
1	1	1	1	0	1	FDh	Inhibited
1	1	1	1	1	0	FEh	Inhibited
1	1	1	1	1	1	FFh	Inhibited

VGL_S [5:0]							
D5	D4	D3	D2	D1	D0	HEX	Value (V)
0	0	0	0	0	0	00h	-6V
0	0	0	0	0	1	01h	-6.2V
0	0	0	0	1	0	02h	-6.4V
0	0	0	0	1	1	03h	-6.6V
0	0	0	1	0	0	04h	-6.8V
…	…	…	…	…	…	…	…
0	1	0	0	1	0	12h	-9.6V
0	1	0	0	1	1	13h	-9.8V
0	1	0	1	0	0	14h	-10V
0	1	0	1	0	1	15h	-10.2V
0	1	0	1	1	0	16h	-10.4V
…	…	…	…	…	…	…	…
1	1	0	0	0	1	31h	-15.8V
1	1	0	0	1	0	32h	-16V
1	1	0	0	1	1	33h	Inhibited
…	…	…	…	…	…	…	…
1	1	1	1	1	1	3Fh	Inhibited

8.3.10 BIST

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCON_CLK		1	1	0	0	0	0	0	0	C0
Parameter	1	0	0	0	1	0	0	0	BIST_ON	10h
	2	BIST_IMG_SEL[15:8]								FFH
	3	BIST_IMG_SEL[7:0]								FFH

H/W reset Default value

Parameter	Value
BIST_ON	00h
BIST_IMG_SEL[15:8]	FFh
BIST_IMG_SEL[70]	FFh

Description

BIST_ON	Set BIST function
BIST_IMG_SEL[15:0]	Set BIST display patterns

Function

BIST_IMG_SEL[7:0]									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**	**Pattern**
0	0	0	0	0	0	0	1	01h	Red
0	0	0	0	0	0	1	0	02h	Green
0	0	0	0	0	1	0	0	04h	Blue
0	0	0	0	1	0	0	0	08h	White
0	0	0	1	0	0	0	0	10h	Black
0	0	1	0	0	0	0	0	20h	V255 Gray
0	1	0	0	0	0	0	0	40h	H255 Gray
1	0	0	0	0	0	0	0	80h	Color bar

BIST_IMG_SEL[15:8]									
D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**HEX**	**Pattern**
0	0	0	0	0	0	0	1	01h	Cross-talk-1
0	0	0	0	0	0	1	0	02h	Cross-talk-2
0	0	0	0	0	1	0	0	04h	64*64 check
0	0	0	0	1	0	0	0	08h	Column Flick
0	0	0	1	0	0	0	0	10h	1-dot Flick
0	0	1	0	0	0	0	0	20h	2-dot Flick
0	1	0	0	0	0	0	0	40h	Red border
1	0	0	0	0	0	0	0	80h	SD CP pattern

8.3.11 TCON

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
TCON		1	1	0	0	0	0	0	1	C1h
Parameter	1	0	0	VBP[9:8]		0	0	VFP[9:8]		00h
	2	VBP[7:0]								0Ch
	3	VFP[7:0]								10h
	4	VSA[7:0]								04h
	5	0	0	HBP[9:8]		0	0	HFP[9:8]		00h
	6	HBP[7:0]								0Ch
	7	HFP[7:0]								10h
	8	HSA[7:0]								04h

H/W reset Default value

Parameter	Value
VBP[9:0]	0Ch
VFP[9:0]	10h
VSA[7:0]	04h
HBP[9:0]	0Ch
HFP[9:0]	10h
HSA[7:0]	04h

Description

VBP[9:0]	Set Vertical back porch.
VFP[9:0]	Set Vertical front porch.
VSA[7:0]	Set Vertical-sync low pulse width
HBP[9:0]	Set Horizontal back porch
HFP[9:0]	Set Horizontal front porch
HSA[7:0]	Set Horizontal-sync low pulse width

Function

VSA[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	Line(HS)
0	0	0	0	0	0	0	0	00h	Disable
0	0	0	0	0	0	0	1	01h	Disable
0	0	0	0	0	0	1	0	02h	2
0	0	0	0	0	0	1	1	03h	3
0	0	0	0	0	1	0	0	04h	4
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	1	FDh	253
1	1	1	1	1	1	1	0	FEh	254
1	1	1	1	1	1	1	1	FFh	255

VBP[9:0] ,VFP[9:0]											
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Line(HS)
0	0	0	0	0	0	0	0	0	0	000h	Disable
0	0	0	0	0	0	0	0	0	1	001h	Disable
0	0	0	0	0	0	0	0	1	0	002h	2
0	0	0	0	0	0	0	0	1	1	003h	3
0	0	0	0	0	0	0	1	0	0	004h	4
…	…	…	…	…	…	…	…	…	…	…	…
0	0	1	1	1	1	1	1	0	1	0FDh	253
0	0	1	1	1	1	1	1	1	0	0FEh	254
0	0	1	1	1	1	1	1	1	1	0FFh	255
…	…	…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1	0	3FEh	1022
1	1	1	1	1	1	1	1	1	1	3FFh	1023

HSA[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	DOT CLK
0	0	0	0	0	0	0	0	00h	Disable
…	…	…	…	…	…	…	…	…	…
0	0	0	0	1	1	1	1	0Fh	Disable
0	0	0	1	0	0	0	0	10h	16 Clock
0	0	0	1	0	0	0	1	11h	17 Clock
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	1	FDh	253 Clock
1	1	1	1	1	1	1	0	FEh	254 Clock
1	1	1	1	1	1	1	1	FFh	255 Clock

HBP[9:0], HFP[9:0]											
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
0	0	0	0	0	0	0	0	0	0	00h	Disable
…	…	…	…	…	…	…	…	…	…	…	…
0	0	0	0	0	0	1	1	1	1	0Fh	Disable
0	0	0	0	0	1	0	0	0	0	10h	16 Clock
…	…	…	…	…	…	…	…	…	…	…	…
0	0	1	1	1	1	1	1	0	1	0FDh	253 Clock
0	0	1	1	1	1	1	1	1	0	0FEh	254 Clock
0	0	1	1	1	1	1	1	1	1	0FFh	255 Clock
…	…	…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1	0	3FEh	1022 Clock
1	1	1	1	1	1	1	1	1	1	3FFh	1023 Clock

8.3.12 TCON_2

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
TCON_2		1	1	0	0	0	0	1	0	C2h
Parameter	1	0	0	NL[9:8]		0	RSO[2:0]			20h
	2	NL[7:0]								80h

H/W reset Default value

Parameter	Value
RSO[2:0]	00h
NL[9:0]	280h

Description

RSO[2:0]	Set Display resolution
NL[9:0]	Set Display resolution, register step is 2 HS.

Function

RSO [2:0]				
D2	D1	D0	HEX	Resolution
0	0	0	0h	720 RGB
0	0	1	1h	600 RGB
0	1	0	2h	640 RGB
0	1	1	3h	Inhibited
1	0	0	4h	Inhibited
1	0	1	5h	Inhibited
1	1	0	6h	Inhibited
1	1	1	7h	Inhibited

NL[9:0]											
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	HEX	Resolution
0	0	0	0	0	0	0	0	0	0	000h	Disable
0	0	0	0	0	0	0	0	0	1	001h	2HS
…	…	…	…	…	…	…	…	…	…	…	…
1	0	1	0	0	0	0	0	0	0	280h	1280HS
…	…	…	…	…	…	…	…	…	…	…	…
1	0	1	1	0	1	0	0	0	0	2D0h	1440HS
…	…	…	…	…	…	…	…	…	…	…	…
1	1	0	1	1	1	0	0	0	0	370h	1760HS
1	1	0	1	1	1	0	0	0	1	371h	Inhibited
…	…	…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	1	1	3FFh	Inhibited

8.3.13 TCON_3

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
TCON_3		1	1	0	0	0	0	1	1	C3h
Parameter	1	0	I2O_BLKF_S[2:0]			BLK_KP	O2I_BLKF_S[2:0]			22h
	2	REV_EOR	B4_EOR	B3_EOR	B2_EOR	0	0	0	0	00h

H/W reset Default value

Parameter	Value
I2O_BLKF_S[2:0]	02h
O2I_BLKF_S[2:0]	02h
BLK_KP	00h
REV_EOR	00h
B4_EOR	00h
B3_EOR	00h
B2_EOR	00h

Description

I2O_BLKF_S[2:0]	Set Sleep-in to sleep-out blanking frame time
O2I_BLKF_S[2:0]	Set Sleep-out to sleep-in blanking frame time
BLK_KP	Set blanking display in display off state.
REV_EOR	Exclusive OR Command INVON.
B4_EOR	Exclusive OR Command MADTCL D4 function.
B3_EOR	Exclusive OR Command MADTCL D3 function.
B2_EOR	Exclusive OR Command MADTCL D2 function.

Function

I2O_BLKF_S[2:0] / O2I_BLKF_S[2:0]				
D2	D1	D0	HEX	Blanking frame
0	0	0	0h	No blanking
0	0	1	1h	1 frame
0	1	0	2h	2 frame
0	1	1	3h	3 frame
1	0	0	4h	4 frame
1	0	1	5h	5 frame
1	1	0	6h	6 frame
1	1	1	7h	7 frame

REV_EOR	INVON	Display
0	0	Normal Display
0	1	Inversion Display
1	0	Inversion Display
1	1	Normal Display

B4_EOR	MADTCL D4 (ML)	Display
0	0	Top → Bottom
0	1	Bottom → Top
1	0	Bottom → Top
1	1	Top → Bottom

B3_EOR	MADTCL D3 (RGB)	Display
0	0	RGB order
0	1	BGR order
1	0	BGR order
1	1	RGB order

B2_EOR	MADTCL D2 (MH)	Display
0	0	Left → Right
0	1	Right → Left
1	0	Right → Left
1	1	Left → Right

8.3.14 DSTB

<table>
<tr><th colspan="2">Inst / Para</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>HEX</th></tr>
<tr><td colspan="2">DSTB</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>C4h</td></tr>
<tr><td>Parameter</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>DSTB</td><td>00h</td></tr>
<tr><td>H/W reset Default value</td><td colspan="10"><table><tr><th>Parameter</th><th>Value</th></tr><tr><td>DSTB</td><td>00h</td></tr></table></td></tr>
<tr><td>Description</td><td colspan="2">DSTB</td><td colspan="8">Set Deep standby mode enable</td></tr>
<tr><td>Function</td><td colspan="10"><table><tr><th>DSTB_ON</th><th>Status</th></tr><tr><td>0h</td><td>Deep standby mode disable</td></tr><tr><td>1h</td><td>Deep standby mode enable</td></tr></table>
Note: Only using Hardware RESET to exit DSTB mode, and the Reset low pulse width needs ≥10 ms</td></tr>
</table>

8.3.15 SRC_TIM

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
SRC_TIM		1	1	0	0	0	1	1	0	C6h
Parameter	1	SD1[7:0]								00h
	2	SD2[7:0]								00h
	3	SD3[7:0]								FFh
	4	OP_ON1[7:0]								00h
	5	OP_ON2[7:0]								00h
	6	1	1	1	1	1	1	1	1	FFh
	7	0	0	0	0	0	0	0	0	00h
	8	0	0	0	0	0	0	0	1	01h

H/W reset Default value

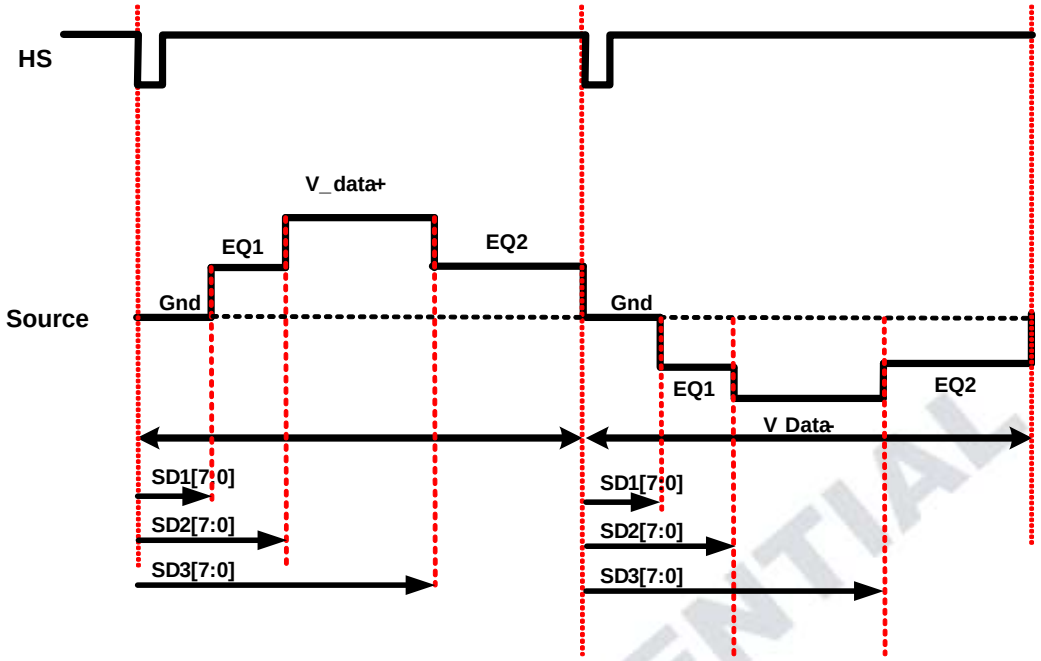
Parameter	Value
SD1[7:0]	00h
SD2[7:0]	00h
SD3[7:0]	FFh
OP_ON1[7:0]	00h
OP_ON2[7:0]	00h

Description

SD1[7:0]	Set EQ pull GND time. Register step is 4x osc clock.
SD2[7:0]	Set EQ pre-charge to VCI or VCL time. Register step is 4x osc clock.
SD3[7:0]	Set Source Data output time. Register step is 4x osc clock.
OP_ON1[7:0]	Set Source OP enable time. Register step is 4x osc clock.
OP_ON2[7:0]	Set Source OP disable time. Register step is 4x osc clock.

Function

SD1[7:0], SD2[7:0], SD3[7:0], OP_ON1[7:0] ; OP_OFF1[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	CLK (Clock)
0	0	0	0	0	0	0	0	00h	0
0	0	0	0	0	0	0	1	01h	4
0	0	0	0	0	0	1	0	02h	8
…	…	…	…	…	…	…	…	…	…
0	0	0	0	1	1	0	0	0C	48
0	0	0	0	1	1	0	1	0D	52
0	0	0	0	1	1	1	0	0E	56
0	0	0	0	1	1	1	1	0F	60
0	0	0	1	0	0	0	0	10	64
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	1	1	FFh	1020



Note 1: Oscillator = 50MHz.

Note2: EQ2 time = 1HS – SD3[7:0].

8.3.16 SRCCON

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
SRCCON		1	1	0	0	0	1	1	1	C7h
Parameter	1	0	1	0	0	0	INV_SEL[2:0]			45h
	2	0	0	1	0	1	0	1	1	2Bh
	3	0	1	0	0	Z_Shift	Z_Line	0	1	41h
	4	PORCH_HIZ	PORCH_GND	SDSW_DATA	SDPORCH_DATA	0	0	0	0	00h
	5	0	0	0	0	0	0	1	0	02h

H/W reset Default value

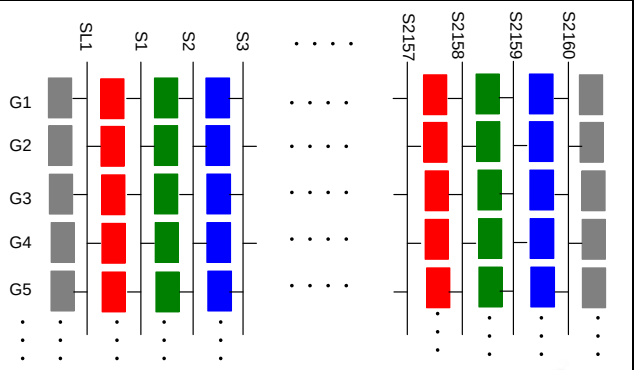
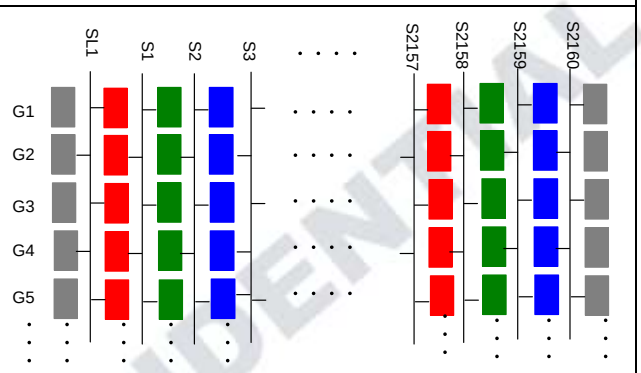
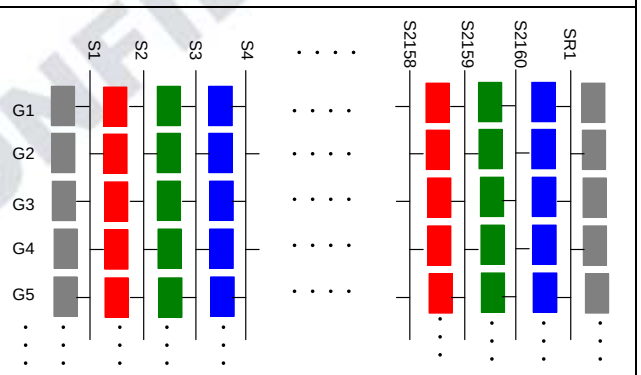
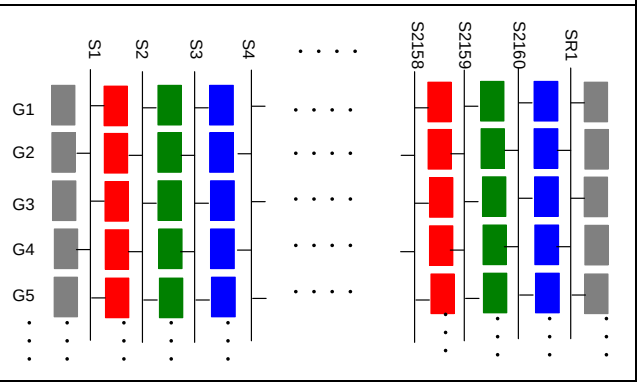
Parameter	Value
Z_Shift	00h
Z_Line	00h
INV_SEL[2:0]	05h
PORCH_HIZ	00h
PORCH_GND	00h
SDSW_DATA	00h
SDPORCH_DATA	00h
SMEQOFF	00h

Description

INV_SEL[2:0]	Sets the inversion type.
Z_shift	Option of Zig-Zag Panel Type, for 1st data setting
Z_line	Option of Zig-Zag Panel Type, for Dummy line setting
PORCH_HIZ	Set Non display area source state.
PORCH_GND	Set Non display area source state.
SDSW_DATA	Set Non display area source state.
SDPORCH_DATA	Set Blanking frame source state.
SMEQOFF	Smart EQ control.

Function

INV_SEL[2:0]				
D2	D1	D0	HEX	Inversion type
0	0	0	00h	1 dot inversion
0	0	1	01h	(Reserved)
0	1	0	02h	2 dot inversion
0	1	1	03h	4 dot inversion
1	0	0	04h	8 dot inversion
1	0	1	05h	Column inversion
1	1	0	06h	Zig-Zag inversion
1	1	1	07h	(Reserved)

Z_SHIFT	Z_LINE	Referenced panel diagram
0	0	
0	1	
1	0	
1	1	

PORCH_HZ	Status
0h	GND / V0 / V255
1h	HZ / GND

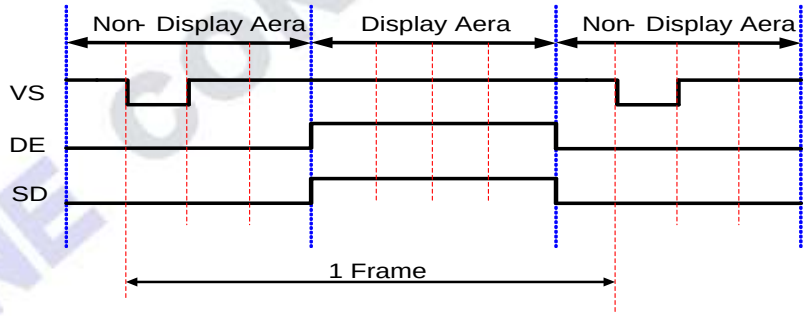
PORCH_GND	Status
0h	GND / V0 / V255
1h	GND

SDPORCH_DATA	Status
0h	V0
1h	V255

SDSW_DATA	Status
0h	V0
1h	V255

SMEQOFF	Status
0h	Enable
1h	Disable

Note : Non-display area and Display area relationship shown as below figure:



8.3.17 SET_GAMMA

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
SET_GAMMA		1	1	0	0	1	0	0	0	C8h
Parameter	1	0	P18[6:0]							7Ch
	2	0	P17[6:0]							6Dh
	3	0	P16[6:0]							63h
	4	0	P15[6:0]							59h
	5	0	P14[6:0]							57h
	6	0	P13[6:0]							4Ah
	7	0	P12[6:0]							51h
	8	0	P11[6:0]							3Ah
	9	0	P10[6:0]							55h
	10	0	P9[6:0]							53h
	11	0	P8[6:0]							55h
	12	0	P7[6:0]							7Ah
	13	0	P6[6:0]							6Fh
	14	0	P5[6:0]							7Fh
	15	0	P4[6:0]							75h
	16	0	P3[6:0]							72h
	17	0	P2[6:0]							62h
	18	0	P1[6:0]							2Dh
	19	0	P0[6:0]							06h
	20	0	N18[6:0]							7Ch
	21	0	N17[6:0]							6Dh
	22	0	N16[6:0]							63h
	23	0	N15[6:0]							59h
	24	0	N14[6:0]							57h
	25	0	N13[6:0]							4Ah
	26	0	N12[6:0]							51h
	27	0	N11[6:0]							3Ah
	28	0	N10[6:0]							55h
	29	0	N9[6:0]							53h
	30	0	N8[6:0]							55h
	31	0	N7[6:0]							7Ah
	32	0	N6[6:0]							6Fh
	33	0	N5[6:0]							7Fh
	34	0	N4[6:0]							75h
	35	0	N3[6:0]							72h
	36	0	N2[6:0]							62h
	37	0	N1[6:0]							2Dh
	38	0	N0[6:0]							06h

Description	P0[6:0] ~ P18[6:0]	Set Positive gamma voltage.
	N0[6:0] ~ N18[6:0]	Set negative gamma voltage.

Function

Gamma point		Gray level	
		Normally black panel	Normally White panel
Positive Gamma setting	P18[6:0]	255	0
	P17[6:0]	251	4
	P16[6:0]	247	8
	P15[6:0]	243	12
	P14[6:0]	235	20
	P13[6:0]	227	28
	P12[6:0]	211	44
	P11[6:0]	191	64
	P10[6:0]	159	96
	P9[6:0]	128	128
	P8[6:0]	96	159
	P7[6:0]	64	191
	P6[6:0]	44	211
	P5[6:0]	28	227
	P4[6:0]	20	235
	P3[6:0]	12	243
	P2[6:0]	8	247
	P1[6:0]	4	251
	P0[6:0]	0	255
Negative gamma setting	N18[6:0]	255	0
	N17[6:0]	251	4
	N16[6:0]	247	8
	N15[6:0]	243	12
	N14[6:0]	235	20
	N13[6:0]	227	28
	N12[6:0]	211	44
	N11[6:0]	191	64
	N10[6:0]	159	96
	N9[6:0]	128	128
	N8[6:0]	96	159
	N7[6:0]	64	191
	N6[6:0]	44	211
	N5[6:0]	28	227
	N4[6:0]	20	235
	N3[6:0]	12	243
	N2[6:0]	8	247
	N1[6:0]	4	251
	N0[6:0]	0	255

8.3.18 OTP_AUTO_PROG

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
OTP_AUTO_PROG		1	1	0	0	1	0	1	1	CBh
Parameter	1	OTP_PROG_BANK[7:0]								00h
	2	OTP_PROG_BANK[15:8]								00h
	3	0	0	0	0	0	0	0	OTP_INT_VPP	00h
	4	1	0	0	0	0	0	0	OTP_AUTO_PROG	80h

H/W reset Default value

Parameter	Value
OTP_PROG_BANK[7:0]	00h
OTP_PROG_BANK[15:8]	00h
OTP_INT_VPP	00h
OTP_AUTO_PROG	00h

Description

OTP_PROG_BANK[15:0]	Set programming OTP banks.
OTP_INT_VPP	Set internal Auto-OTP power
OTP_AUTO_PROG	Set OTP cell program. (.)

Function

OTP_INT_VPP	Status
00h	Using external power (VPP)
01h	Using internal power (OTP_VGH_S[5:0])

OTP_AUTO_PROG	Status
00h	Disable
01h	Enable

Note: See Sec 6.5_OTP Programing Flow, for detail description

8.3.19 ETC

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
ETC		1	1	0	1	0	0	0	0	D0h
Parameter	1	0	0	0	0	BATON_HS	1	1	FS_EN	07h
	2	FS_DETECT[7:0]								10h
	3	BATON_CNT[7:0]								10h

H/W reset Default value

Parameter	Value
FS_EN	01h
BATON_HS	00h
FS_DETECT[7:0]	10h
BATON_CNT[7:0]	10h

Description

FS_EN	Set MIPI abnormal function.
BATON_HS	Using HS unit to set detect time entering power-abnormal status.
FS_DETECT[7:0]	Set detect time to enter MIPI-abnormal status. Register step is 1.28us.
BATON_CNT[7:0]	Set detect time to enter power-abnormal status. Register step is 0.08us.

Function

BATON_HS	Status
00h	BATON_CNT basing is Internal OSC.
01h	BATON_CNT basing is HS.

FS_DETECT[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	Value (us)
0	0	0	0	0	0	0	0	00h	0
0	0	0	0	0	0	0	1	01h	1.28
0	0	0	0	0	0	1	0	02h	2.56
0	0	0	0	0	0	1	1	03h	3.84
0	0	0	0	0	1	0	0	04h	5.12
…	…	…	…	…	…	…	…	…	…
0	0	0	0	1	1	1	1	0Fh	11.52
0	0	0	1	0	0	0	0	10h	12.8
0	0	0	1	0	0	0	1	11h	14.08
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	0	1	0	FAh	320
1	1	1	1	1	0	1	1	FBh	321.28
1	1	1	1	1	1	0	0	FCh	322.56
1	1	1	1	1	1	0	1	FDh	323.84
1	1	1	1	1	1	1	0	FEh	325.12
1	1	1	1	1	1	1	1	FFh	326.4

BATON_CNT[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	Value (us)
0	0	0	0	0	0	0	0	00h	0
0	0	0	0	0	0	0	1	01h	0.08
0	0	0	0	0	0	1	0	02h	0.16
0	0	0	0	0	0	1	1	03h	0.24
0	0	0	0	0	1	0	0	04h	0.32
…	…	…	…	…	…	…	…	…	…
0	0	0	0	1	1	1	1	0Fh	0.72
0	0	0	1	0	0	0	0	10h	0.8
0	0	0	1	0	0	0	1	11h	0.88
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	0	1	0	FAh	20
1	1	1	1	1	0	1	1	FBh	20.08
1	1	1	1	1	1	0	0	FCh	20.16
1	1	1	1	1	1	0	1	FDh	20.24
1	1	1	1	1	1	1	0	FEh	20.32
1	1	1	1	1	1	1	1	FFh	20.4

8.3.20 CABC_CTR

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABC_CTR		1	1	1	0	0	0	0	0	E0h
Parameter	1	0	0	1	1	PWM_POL	0	0	0	30h
	2	BCFRQSEL[7:0]								29h
	3	0	0	1	0	0	0	0	1	21h
	4	0	PFSTEP[2:0]			0	DFSTEP[2:0]			10h
	5	0	0	PWMSTEP[5:0]						1Fh
	6	0	0	0	0	0	1	1	0	06h
	7	0	1	1	0	0	0	1	0	62h
	8	0	DBV_SEL	0	1	1	1	1	1	1Fh
	9	1	0	1	0	0	0	0	0	A0h
	10	DATASTEP[3:0]				0	1	0	0	14h
	11	1	1	0	0	1	1	0	0	CCh
	12	0	0	0	0	0	0	0	0	00h
	13	TGN0_00[7:0]								FFh
	14	TGN0_01[7:0]								FAh
	15	TGN0_02[7:0]								FDh
	16	TGN0_03[7:0]								F0h
	17	TGN0_04[7:0]								FDh
	18	TGN0_05[7:0]								F8h
	19	TGN0_06[7:0]								FDh
	20	TGN0_07[7:0]								F8h
	21	TGN0_08[7:0]								FAh
	22	TGN0_09[7:0]								FCh
	23	TGN0_10[7:0]								FCh
	24	TGN0_11[7:0]								F0h
	25	TGN0_12[7:0]								FFh

H/W reset Default value

Parameter	Value
PWM_POL	00h
BCFRQSEL[7:0]	29h
PFSTEP[2:0]	01h
PWMSTEP[5:0]	1Fh
DFSTEP[2:0]	00h
DATASTEP[3:0]	10h
DBV_SEL	00h

Description

PWM_POL	Set CABC_PWM_OUT signal polarity.
BCFRQSEL[7:0]	Set PWM frequency. Register step 120Hz.
PFSTEP[2:0]	Set the frame counts of PWM dimming.
PWMSTEP[5:0]	Set PWM dimming step per frame.

	DFSTEP[2:0]	Set the frame counts of CABC-data dimming.
	DATASTEP[3:0]	Set Data dimming step per frame.
	DBV_SEL	Set the PWM duty with 8bit or 12bit input command.
	TGN0_00[7:0]~ TGN0_12[7:0]	Set data gain for CABC UI (User Interface) Image mode.

Function

PWM_POL	Status
0h	Original
1h	Inversed

BCFRQSEL[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	PWM Freq.(Hz)
0	0	0	0	0	0	0	0	00h	120
0	0	0	0	0	0	0	1	01h	240
0	0	0	0	0	0	1	0	02h	360
0	0	0	0	0	0	1	1	03h	480
…	…	…	…	…	…	…	…	…	…
0	0	1	0	0	1	1	1	27h	4800
0	0	1	0	1	0	0	0	28h	4920
0	0	1	0	1	0	0	1	29h	5040
0	0	1	0	1	0	1	0	2Ah	5160
0	0	1	0	1	0	1	1	2Bh	5280
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	1	FDh	30480
1	1	1	1	1	1	1	0	FEh	30600
1	1	1	1	1	1	1	1	FFh	30720

Note: Calculated at Display frame rate is 60Hz.

PFSTEP[2:0]				
D2	D1	D0	HEX	Changed frame of PWM dimming
0	0	0	0h	1 frame
0	0	1	1h	2 frame
0	1	0	2h	4 frame
0	1	1	3h	8 frame
1	0	0	4h	16 frame
1	0	1	5h	32 frame
1	1	0	6h	64 frame
1	1	1	7h	128 frame

PWMSTEP[5:0]							
D5	D4	D3	D2	D1	D0	HEX	PWM-changed Step per frame
0	0	0	0	0	0	00h	0 step
0	0	0	0	0	1	01h	1 step
0	0	0	0	1	0	02h	2 steps
0	0	0	0	1	1	03h	3 steps
…	…	…	…	…	…	…	…
1	1	1	1	0	1	61h	61 steps
1	1	1	1	1	0	62h	62 steps
1	1	1	1	1	1	63h	63 steps

DFSTEP[2:0]				
D2	D1	D0	HEX	Changed frame of Data dimming
0	0	0	0h	1 frame
0	0	1	1h	2 frame
0	1	0	2h	4 frame
0	1	1	3h	8 frame
1	0	0	4h	16 frame
1	0	1	5h	32 frame
1	1	0	6h	64 frame
1	1	1	7h	128 frame

DATASTEP[3:0]					
D3	D2	D1	D0	HEX	Data-changed Step per frame
0	0	0	0	00h	0 step
0	0	0	1	01h	1 step
0	0	1	0	02h	2 steps
0	0	1	1	03h	3 steps
…	…	…	…	…	…
1	1	0	0	12h	12 steps
1	1	0	1	13h	13 steps
1	1	1	0	14h	14 steps
1	1	1	1	15h	15 steps

DBV_SEL	Status
0h	Using 12-bit setting of Display Brightness.
1h	Using 8-bit setting of Display Brightness.

TGN0_00[7:0]~ TGN0_12[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	CABC gain
0	0	0	0	0	0	0	0	00h	Inhibited
0	0	0	0	0	0	0	1	01h	1+α
0	0	0	0	0	0	1	0	02h	1+α/2
0	0	0	0	0	0	1	1	03h	1+α/3
…	…	…	…	…	…	…	…	…	…
0	0	1	0	0	1	1	1	27h	1+α/27
0	0	1	0	1	0	0	0	28h	1+α/28
0	0	1	0	1	0	0	1	29h	1+α/29
0	0	1	0	1	0	1	0	2Ah	1+α/30
0	0	1	0	1	0	1	1	2Bh	1+α/31
…	…	…	…	…	…	…	…	…	…
1	1	1	1	1	1	0	1	FDh	1+α/253
1	1	1	1	1	1	1	0	FEh	1+α/254
1	1	1	1	1	1	1	1	FFh	1+α/255

Note: “α” is a variable of Chipone’s CABC algorithm to fit display quality.

8.3.21 CABC_SET_1

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABC_SET_1		1	1	1	0	0	0	0	1	E1h
Parameter	1	TGN1_00[7:0]								AFh
	2	TGN1_01[7:0]								C8h
	3	TGN1_02[7:0]								EAh
	4	TGN1_03[7:0]								E6h
	5	TGN1_04[7:0]								E4h
	6	TGN1_05[7:0]								CCh
	7	TGN1_06[7:0]								E4h
	8	TGN1_07[7:0]								BEh
	9	TGN1_08[7:0]								F0h
	10	TGN1_09[7:0]								B2h
	11	TGN1_10[7:0]								BEh
	12	TGN1_11[7:0]								C6h
	13	TGN1_12[7:0]								FFh
	14	TGN2_00[7:0]								AFh
	15	TGN2_01[7:0]								C8h
	16	TGN2_02[7:0]								E9h
	17	TGN2_03[7:0]								E5h
	18	TGN2_04[7:0]								E3h
	19	TGN2_05[7:0]								CBh
	20	TGN2_06[7:0]								E3h
	21	TGN2_07[7:0]								BEh
	22	TGN2_08[7:0]								EFh
	23	TGN2_09[7:0]								B2h
	24	TGN2_10[7:0]								BEh
	25	TGN2_11[7:0]								C6h
	26	TGN2_12[7:0]								FFh
Description	TGN1_00[7:0]~ TGN1_12[7:0]	Set data gain for CABC still-picture mode.								
	TGN2_00[7:0]~ TGN2_12[7:0]	Set data gain for CABC moving-image mode.								

Function

TGN1_00[7:0]~TGN1_12[7:0], TGN2_00[7:0]~ TGN2_12[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	CABC gain
0	0	0	0	0	0	0	0	00h	Inhibited
0	0	0	0	0	0	0	1	01h	1+α
0	0	0	0	0	0	1	0	02h	1+α/2
0	0	0	0	0	0	1	1	03h	1+α/3
…	…	…	…	…	…	…	…	…	
0	0	1	0	0	1	1	1	27h	1+α/27
0	0	1	0	1	0	0	0	28h	1+α/28

0	0	1	0	1	0	0	1	29h	1+α/29
0	0	1	0	1	0	1	0	2Ah	1+α/30
0	0	1	0	1	0	1	1	2Bh	1+α/31
…	…	…	…	…	…	…	…	…	
1	1	1	1	1	1	0	1	FDh	1+α/253
1	1	1	1	1	1	1	0	FEh	1+α/254
1	1	1	1	1	1	1	1	FFh	1+α/255

Note **:** "α" is a variable of Chipone's CABC algorithm to fit display quality.

8.3.22 CABCPWM_SET_1

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABCPWM_SET_1		1	1	1	0	0	0	1	0	E2h
Parameter	1	BCRECY0_01[11:8]				BCRECY0_00[11:8]				EFh
	2	BCRECY0_03[11:8]				BCRECY0_02[11:8]				EFh
	3	BCRECY0_05[11:8]				BCRECY0_04[11:8]				EFh
	4	BCRECY0_07[11:8]				BCRECY0_06[11:8]				EFh
	5	BCRECY0_09[11:8]				BCRECY0_08[11:8]				EFh
	6	BCRECY0_11[11:8]				BCRECY0_10[11:8]				EFh
	7	0	0	0	0	BCRECY0_12[11:8]				0Fh
	8	BCRECY0_00[7:0]								80h
	9	BCRECY0_01[7:0]								D0h
	10	BCRECY0_02[7:0]								00h
	11	BCRECY0_03[7:0]								00h
	12	BCRECY0_04[7:0]								00h
	13	BCRECY0_05[7:0]								C0h
	14	BCRECY0_06[7:0]								00h
	15	BCRECY0_07[7:0]								C0h
	16	BCRECY0_08[7:0]								00h
	17	BCRECY0_09[7:0]								F0h
	18	BCRECY0_10[7:0]								F0h
	19	BCRECY0_11[7:0]								00h
	20	BCRECY0_12[7:0]								80h
Description	BCRECY0_0[7:0]~BCRECY0_12[7:0]	Set PWM gain for CABC UI (User Interface) Image mode.								

Function

BCRECY0_0[7:0] ~ BCRECY0_12[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	CABC gain
0	0	0	0	0	0	0	0	00h	Inhibited
0	0	0	0	0	0	0	1	01h	β
0	0	0	0	0	0	1	0	02h	2*β
0	0	0	0	0	0	1	1	03h	3*β
…	…	…	…	…	…	…	…	…	
0	0	1	0	0	1	1	1	27h	27*β
0	0	1	0	1	0	0	0	28h	28*β
0	0	1	0	1	0	0	1	29h	29*β
…	…	…	…	…	…	…	…	…	
1	1	1	1	1	1	0	1	FDh	253*β
1	1	1	1	1	1	1	0	FEh	254*β
1	1	1	1	1	1	1	1	FFh	255*β

Note: "β" is "WRDISBV" setting value.

8.3.23 CABCPWM_SET_2

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABCPWM_SET_2		1	1	1	0	0	0	1	1	E3h
Parameter	1	BCRECY1_01[11:8]				BCRECY1_00[11:8]				98h
	2	BCRECY1_03[11:8]				BCRECY1_02[11:8]				9Eh
	3	BCRECY1_05[11:8]				BCRECY1_04[11:8]				BCh
	4	BCRECY1_07[11:8]				BCRECY1_06[11:8]				Ach
	5	BCRECY1_09[11:8]				BCRECY1_08[11:8]				9Bh
	6	BCRECY1_11[11:8]				BCRECY1_10[11:8]				79h
	7	0	0	0	0	BCRECY1_12[11:8]				0Fh
	8	BCRECY1_00[7:0]								F0h
	9	BCRECY1_01[7:0]								80h
	10	BCRECY1_02[7:0]								30h
	11	BCRECY1_03[7:0]								00h
	12	BCRECY1_04[7:0]								80h
	13	BCRECY1_05[7:0]								00h
	14	BCRECY1_06[7:0]								80h
	15	BCRECY1_07[7:0]								00h
	16	BCRECY1_08[7:0]								E0h
	17	BCRECY1_09[7:0]								60h
	18	BCRECY1_10[7:0]								60h
	19	BCRECY1_11[7:0]								FFh
	20	BCRECY1_12[7:0]								D0h
Description		BCRECY1_0[7:0]~BCRECY1_12[7:0]				Set PWM gain for CABC still-picture mode.				

Function

BCRECY1_0[7:0] ~ BCRECY1_12[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	CABC gain
0	0	0	0	0	0	0	0	00h	Inhibited
0	0	0	0	0	0	0	1	01h	β
0	0	0	0	0	0	1	0	02h	2*β
0	0	0	0	0	0	1	1	03h	3*β
…	…	…	…	…	…	…	…	…	
0	0	1	0	0	1	1	1	27h	27*β
0	0	1	0	1	0	0	0	28h	28*β
0	0	1	0	1	0	0	1	29h	29*β
…	…	…	…	…	…	…	…	…	
1	1	1	1	1	1	0	1	FDh	253*β
1	1	1	1	1	1	1	0	FEh	254*β
1	1	1	1	1	1	1	1	FFh	255*β

Note: "β" is "WRDISBV" setting value.

8.3.24 CABCPWM_SET_3

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
CABCPWM_SET_3		1	1	1	0	0	1	0	0	E4h
Parameter	1	BCRECY2_01[11:8]				BCRECY2_00[11:8]				98h
	2	BCRECY2_03[11:8]				BCRECY2_02[11:8]				8Eh
	3	BCRECY2_05[11:8]				BCRECY2_04[11:8]				ACh
	4	BCRECY2_07[11:8]				BCRECY2_06[11:8]				ACh
	5	BCRECY2_09[11:8]				BCRECY2_08[11:8]				9Bh
	6	BCRECY2_11[11:8]				BCRECY2_10[11:8]				79h
	7	0	0	0	0	BCRECY2_12[11:8]				0Fh
	8	BCRECY2_00[7:0]								E0h
	9	BCRECY2_01[7:0]								70h
	10	BCRECY2_02[7:0]								20h
	11	BCRECY2_03[7:0]								F0h
	12	BCRECY2_04[7:0]								70h
	13	BCRECY2_05[7:0]								F0h
	14	BCRECY2_06[7:0]								70h
	15	BCRECY2_07[7:0]								00h
	16	BCRECY2_08[7:0]								D0h
	17	BCRECY2_09[7:0]								60h
	18	BCRECY2_10[7:0]								50h
	19	BCRECY2_11[7:0]								FFh
	20	BCRECY2_12[7:0]								C0h
Description	BCRECY2_0[7:0]~BCRECY2_12[7:0]	Set PWM gain for CABC moving-image mode.								

Function

BCRECY2_0[7:0] ~ BCRECY_12[7:0]									
D7	D6	D5	D4	D3	D2	D1	D0	HEX	CABC gain
0	0	0	0	0	0	0	0	00h	Inhibited
0	0	0	0	0	0	0	1	01h	β
0	0	0	0	0	0	1	0	02h	2*β
0	0	0	0	0	0	1	1	03h	3*β
…	…	…	…	…	…	…	…	…	
0	0	1	0	0	1	1	1	27h	27*β
0	0	1	0	1	0	0	0	28h	28*β
0	0	1	0	1	0	0	1	29h	29*β
…	…	…	…	…	…	…	…	…	
1	1	1	1	1	1	0	1	FDh	253*β
1	1	1	1	1	1	1	0	FEh	254*β
1	1	1	1	1	1	1	1	FFh	255*β

Note: "β" is "WRDISBV" setting value.

8.3.25 CE_SET

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
CE_SET		1	1	1	0	0	1	0	1	E5h
Parameter	1	0	0	CONST_ON	SKIN_ON	0	SE_ON	HP_ON	0	00h
	2	0	0	0	1	0	0	1	0	12h
	3	0	0	0	0	1	1	1	1	0Fh
	4	1	1	1	1	1	1	1	1	FFh
	5	1	1	1	1	1	1	1	1	FFh
	6	1	1	1	1	1	1	1	1	FFh
	7	0	0	0	0	0	0	0	0	00h
	8	0	0	0	0	0	0	0	0	00h

H/W reset Default value

Parameter	Value
CONST_ON	0h
SKIN_ON	0h
SE_ON	0h
HP_ON	0h

Description

CONST_ON	Set Contrast enhance function
SKIN_ON	Set skin color preservation function
SE_ON	Set Saturation enhance function
HP_ON	Set sharpness enhance function

Function

CONST_ON	Function
0h	Disable Contrast enhance function
1h	Enable Contrast enhance function

SKIN_ON	Function
0h	Disable skin color preservation function
1h	Enable skin color preservation function

SE_ON	Function
0h	Disable Saturation enhance function
1h	Enable Saturation enhance function

HP_ON	Function
0h	Disable sharpness enhance function
1h	Enable sharpness enhance function

8.3.26 DGC_CTRL

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_CTRL		1	1	1	0	0	1	1	1	E7h
Parameter	1	0	0	0	0	0	0	DTR_EN	DGC_EN	00h

H/W reset Default value

Parameter	Value
DTR_EN	0h
DGC_EN	0h

Function

DTR_EN	Function
0h	Disable dithering function
1h	Enable dithering function

DGC_EN	Function
0h	Disable digital gamma function
1h	Enable digital gamma function

8.3.27 DGC_R

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_R		1	1	1	0	1	0	0	0	E8h
Parameter	1	DGC_R_V255[9:2]								FFh
	2	DGC_R_V254[9:2]								FEh
	3	DGC_R_V252[9:2]								FCh
	4	DGC_R_V250[9:2]								FAh
	5	DGC_R_V248[9:2]								F8h
	6	DGC_R_V244[9:2]								F4h
	7	DGC_R_V240[9:2]								F0h
	8	DGC_R_V232[9:2]								E8h
	9	DGC_R_V224[9:2]								E0h
	10	DGC_R_V208[9:2]								D0h
	11	DGC_R_V192[9:2]								C0h
	12	DGC_R_V160[9:2]								A0h
	13	DGC_R_V128[9:2]								80h
	14	DGC_R_V127[9:2]								7Fh
	15	DGC_R_V95[9:2]								5Fh
	16	DGC_R_V63[9:2]								3Fh
	17	DGC_R_V47[9:2]								2Fh
	18	DGC_R_V31[9:2]								1Fh
	19	DGC_R_V23[9:2]								17h
	20	DGC_R_V15[9:2]								0Fh
	21	DGC_R_V11[9:2]								0Bh
	22	DGC_R_V7[9:2]								07h
	23	DGC_R_V5[9:2]								05h
	24	DGC_R_V3[9:2]								03h
	25	DGC_R_V1[9:2]								01h
	26	DGC_R_V0[9:2]								00h

Description		
	DGC_R_V255[9:2]	Set Level_255 of Red data.
	DGC_R_V254[9:2]	Set Level_254 of Red data.
	DGC_R_V252[9:2]	Set Level_252 of Red data.
	DGC_R_V250[9:2]	Set Level_250 of Red data.
	DGC_R_V248[9:2]	Set Level_248 of Red data.
	DGC_R_V244[9:2]	Set Level_244 of Red data.
	DGC_R_V240[9:2]	Set Level_240 of Red data.
	DGC_R_V232[9:2]	Set Level_232 of Red data.
	DGC_R_V224[9:2]	Set Level_224 of Red data.
	DGC_R_V208[9:2]	Set Level_208 of Red data.
	DGC_R_V192[9:2]	Set Level_192 of Red data.
	DGC_R_V160[9:2]	Set Level_160 of Red data.

	DGC_R_V128[9:2]	Set Level_128 of Red data.
	DGC_R_V127[9:2]	Set Level_127 of Red data.
	DGC_R_V95[9:2]	Set Level_95 of Red data.
	DGC_R_V63[9:2]	Set Level_63 of Red data.
	DGC_R_V47[9:2]	Set Level_47 of Red data.
	DGC_R_V31[9:2]	Set Level_31 of Red data.
	DGC_R_V23[9:2]	Set Level_23 of Red data.
	DGC_R_V15[9:2]	Set Level_15 of Red data.
	DGC_R_V11[9:2]	Set Level_11 of Red data.
	DGC_R_V7[9:2]	Set Level_7 of Red data.
	DGC_R_V5[9:2]	Set Level_5 of Red data.
	DGC_R_V3[9:2]	Set Level_3 of Red data.
	DGC_R_V1[9:2]	Set Level_1 of Red data.
	DGC_R_V0[9:2]	Set Level_0 of Red data.

8.3.28 DGC_G

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_R		1	1	1	0	1	0	0	1	E9h
Parameter	1	DGC_G_V255[9:2]								FFh
	2	DGC_G_V254[9:2]								FEh
	3	DGC_G_V252[9:2]								FCh
	4	DGC_G_V250[9:2]								FAh
	5	DGC_G_V248[9:2]								F8h
	6	DGC_G_V244[9:2]								F4h
	7	DGC_G_V240[9:2]								F0h
	8	DGC_G_V232[9:2]								E8h
	9	DGC_G_V224[9:2]								E0h
	10	DGC_G_V208[9:2]								D0h
	11	DGC_G_V192[9:2]								C0h
	12	DGC_G_V160[9:2]								A0h
	13	DGC_G_V128[9:2]								80h
	14	DGC_G_V127[9:2]								7Fh
	15	DGC_G_V95[9:2]								5Fh
	16	DGC_G_V63[9:2]								3Fh
	17	DGC_G_V47[9:2]								2Fh
	18	DGC_G_V31[9:2]								1Fh
	19	DGC_G_V23[9:2]								17h
	20	DGC_G_V15[9:2]								0Fh
	21	DGC_G_V11[9:2]								0Bh
	22	DGC_G_V7[9:2]								07h
	23	DGC_G_V5[9:2]								05h
	24	DGC_G_V3[9:2]								03h
	25	DGC_G_V1[9:2]								01h
	26	DGC_G_V0[9:2]								00h

Description		
	DGC_G_V255[9:2]	Set Level_255 of Green data.
	DGC_G_V254[9:2]	Set Level_254 of Green data.
	DGC_G_V252[9:2]	Set Level_252 of Green data.
	DGC_G_V250[9:2]	Set Level_250 of Green data.
	DGC_G_V248[9:2]	Set Level_248 of Green data.
	DGC_G_V244[9:2]	Set Level_244 of Green data.
	DGC_G_V240[9:2]	Set Level_240 of Green data.
	DGC_G_V232[9:2]	Set Level_232 of Green data.
	DGC_G_V224[9:2]	Set Level_224 of Green data.
	DGC_G_V208[9:2]	Set Level_208 of Green data.
	DGC_G_V192[9:2]	Set Level_192 of Green data.
	DGC_G_V160[9:2]	Set Level_160 of Green data.

	DGC_G_V128[9:2]	Set Level_128 of Green data.
	DGC_G_V127[9:2]	Set Level_127 of Green data.
	DGC_G_V95[9:2]	Set Level_95 of Green data.
	DGC_G_V63[9:2]	Set Level_63 of Green data.
	DGC_G_V47[9:2]	Set Level_47 of Green data.
	DGC_G_V31[9:2]	Set Level_31 of Green data.
	DGC_G_V23[9:2]	Set Level_23 of Green data.
	DGC_G_V15[9:2]	Set Level_15 of Green data.
	DGC_G_V11[9:2]	Set Level_11 of Green data.
	DGC_G_V7[9:2]	Set Level_7 of Green data.
	DGC_G_V5[9:2]	Set Level_5 of Green data.
	DGC_G_V3[9:2]	Set Level_3 of Green data.
	DGC_G_V1[9:2]	Set Level_1 of Green data.
	DGC_G_V0[9:2]	Set Level_0 of Green data.

8.3.29 DGC_B

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_B		1	1	1	0	1	0	1	0	EAh
Parameter	1	DGC_B_V255[9:2]								FFh
	2	DGC_B_V254[9:2]								FEh
	3	DGC_B_V252[9:2]								FCh
	4	DGC_B_V250[9:2]								FAh
	5	DGC_B_V248[9:2]								F8h
	6	DGC_B_V244[9:2]								F4h
	7	DGC_B_V240[9:2]								F0h
	8	DGC_B_V232[9:2]								E8h
	9	DGC_B_V224[9:2]								E0h
	10	DGC_B_V208[9:2]								D0h
	11	DGC_B_V192[9:2]								C0h
	12	DGC_B_V160[9:2]								A0h
	13	DGC_B_V128[9:2]								80h
	14	DGC_B_V127[9:2]								7Fh
	15	DGC_B_V95[9:2]								5Fh
	16	DGC_B_V63[9:2]								3Fh
	17	DGC_B_V47[9:2]								2Fh
	18	DGC_B_V31[9:2]								1Fh
	19	DGC_B_V23[9:2]								17h
	20	DGC_B_V15[9:2]								0Fh
	21	DGC_B_V11[9:2]								0Bh
	22	DGC_B_V7[9:2]								07h
	23	DGC_B_V5[9:2]								05h
	24	DGC_B_V3[9:2]								03h
	25	DGC_B_V1[9:2]								01h
	26	DGC_B_V0[9:2]								00h

Description		
	DGC_B_V255[9:2]	Set Level_255 of Blue data.
	DGC_B_V254[9:2]	Set Level_254 of Blue data.
	DGC_B_V252[9:2]	Set Level_252 of Blue data.
	DGC_B_V250[9:2]	Set Level_250 of Blue data.
	DGC_B_V248[9:2]	Set Level_248 of Blue data.
	DGC_B_V244[9:2]	Set Level_244 of Blue data.
	DGC_B_V240[9:2]	Set Level_240 of Blue data.
	DGC_B_V232[9:2]	Set Level_232 of Blue data.
	DGC_B_V224[9:2]	Set Level_224 of Blue data.
	DGC_B_V208[9:2]	Set Level_208 of Blue data.
	DGC_B_V192[9:2]	Set Level_192 of Blue data.
	DGC_B_V160[9:2]	Set Level_160 of Blue data.

	DGC_B_V128[9:2]	Set Level_128 of Blue data.
	DGC_B_V127[9:2]	Set Level_127 of Blue data.
	DGC_B_V95[9:2]	Set Level_95 of Blue data.
	DGC_B_V63[9:2]	Set Level_63 of Blue data.
	DGC_B_V47[9:2]	Set Level_47 of Blue data.
	DGC_B_V31[9:2]	Set Level_31 of Blue data.
	DGC_B_V23[9:2]	Set Level_23 of Blue data.
	DGC_B_V15[9:2]	Set Level_15 of Blue data.
	DGC_B_V11[9:2]	Set Level_11 of Blue data.
	DGC_B_V7[9:2]	Set Level_7 of Blue data.
	DGC_B_V5[9:2]	Set Level_5 of Blue data.
	DGC_B_V3[9:2]	Set Level_3 of Blue data.
	DGC_B_V1[9:2]	Set Level_1 of Blue data.
	DGC_B_V0[9:2]	Set Level_0 of Blue data.

8.3.30 DGC_R_L

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_R_L		1	1	1	0	1	0	1	1	EBh
Parameter	1	DGC_R_V255[1:0]		DGC_R_V254[1:0]		DGC_R_V252[1:0]		DGC_R_V250[1:0]		00h
	2	DGC_R_V248[1:0]		DGC_R_V244[1:0]		DGC_R_V240[1:0]		DGC_R_V232[1:0]		00h
	3	DGC_R_V224[1:0]		DGC_R_V208[1:0]		DGC_R_V192[1:0]		DGC_R_V160[1:0]		00h
	4	DGC_R_V128[1:0]		DGC_R_V127[1:0]		DGC_R_V95[1:0]		DGC_R_V63[1:0]		00h
	5	DGC_R_V47[1:0]		DGC_R_V31[1:0]		DGC_R_V23[1:0]		DGC_R_V15[1:0]		00h
	6	DGC_R_V11[1:0]		DGC_R_V7[1:0]		DGC_R_V5[1:0]		DGC_R_V3[1:0]		00h
	7	DGC_R_V1[1:0]		DGC_R_V0[1:0]		0	0	0	0	00h

Description	
DGC_R_V255[1:0]	Set Level_255 of Red data.
DGC_R_V254[1:0]	Set Level_254 of Red data.
DGC_R_V252[1:0]	Set Level_252 of Red data.
DGC_R_V250[1:0]	Set Level_250 of Red data.
DGC_R_V248[1:0]	Set Level_248 of Red data.
DGC_R_V244[1:0]	Set Level_244 of Red data.
DGC_R_V240[1:0]	Set Level_240 of Red data.
DGC_R_V232[1:0]	Set Level_232 of Red data.
DGC_R_V224[1:0]	Set Level_224 of Red data.
DGC_R_V208[1:0]	Set Level_208 of Red data.
DGC_R_V192[1:0]	Set Level_192 of Red data.
DGC_R_V160[1:0]	Set Level_160 of Red data.
DGC_R_V128[1:0]	Set Level_128 of Red data.
DGC_R_V127[1:0]	Set Level_127 of Red data.
DGC_R_V95[1:0]	Set Level_95 of Red data.
DGC_R_V63[1:0]	Set Level_63 of Red data.
DGC_R_V47[1:0]	Set Level_47 of Red data.
DGC_R_V31[1:0]	Set Level_31 of Red data.
DGC_R_V23[1:0]	Set Level_23 of Red data.
DGC_R_V15[1:0]	Set Level_15 of Red data.
DGC_R_V11[1:0]	Set Level_11 of Red data.
DGC_R_V7[1:0]	Set Level_7 of Red data.
DGC_R_V5[1:0]	Set Level_5 of Red data.
DGC_R_V3[1:0]	Set Level_3 of Red data.
DGC_R_V1[1:0]	Set Level_1 of Red data.
DGC_R_V0[1:0]	Set Level_0 of Red data.

8.3.31 DGC_G_L

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_R_L		1	1	1	0	1	1	0	0	ECh
Parameter	1	DGC_G_V255[1:0]		DGC_G_V254[1:0]		DGC_G_V252[1:0]		DGC_G_V250[1:0]		00h
	2	DGC_G_V248[1:0]		DGC_G_V244[1:0]		DGC_G_V240[1:0]		DGC_G_V232[1:0]		00h
	3	DGC_G_V224[1:0]		DGC_G_V208[1:0]		DGC_G_V192[1:0]		DGC_G_V160[1:0]		00h
	4	DGC_G_V128[1:0]		DGC_G_V127[1:0]		DGC_G_V95[1:0]		DGC_G_V63[1:0]		00h
	5	DGC_G_V47[1:0]		DGC_G_V31[1:0]		DGC_G_V23[1:0]		DGC_G_V15[1:0]		00h
	6	DGC_G_V11[1:0]		DGC_G_V7[1:0]		DGC_G_V5[1:0]		DGC_G_V3[1:0]		00h
	7	DGC_G_V1[1:0]		DGC_G_V0[1:0]		0	0	0	0	00h

Description	
DGC_G_V255[1:0]	Set Level_255 of Green data.
DGC_G_V254[1:0]	Set Level_254 of Green data.
DGC_G_V252[1:0]	Set Level_252 of Green data.
DGC_G_V250[1:0]	Set Level_250 of Green data.
DGC_G_V248[1:0]	Set Level_248 of Green data.
DGC_G_V244[1:0]	Set Level_244 of Green data.
DGC_G_V240[1:0]	Set Level_240 of Green data.
DGC_G_V232[1:0]	Set Level_232 of Green data.
DGC_G_V224[1:0]	Set Level_224 of Green data.
DGC_G_V208[1:0]	Set Level_208 of Green data.
DGC_G_V192[1:0]	Set Level_192 of Green data.
DGC_G_V160[1:0]	Set Level_160 of Green data.
DGC_G_V128[1:0]	Set Level_128 of Green data.
DGC_G_V127[1:0]	Set Level_127 of Green data.
DGC_G_V95[1:0]	Set Level_95 of Green data.
DGC_G_V63[1:0]	Set Level_63 of Green data.
DGC_G_V47[1:0]	Set Level_47 of Green data.
DGC_G_V31[1:0]	Set Level_31 of Green data.
DGC_G_V23[1:0]	Set Level_23 of Green data.
DGC_G_V15[1:0]	Set Level_15 of Green data.
DGC_G_V11[1:0]	Set Level_11 of Green data.
DGC_G_V7[1:0]	Set Level_7 of Green data.
DGC_G_V5[1:0]	Set Level_5 of Green data.
DGC_G_V3[1:0]	Set Level_3 of Green data.
DGC_G_V1[1:0]	Set Level_1 of Green data.
DGC_G_V0[1:0]	Set Level_0 of Green data.

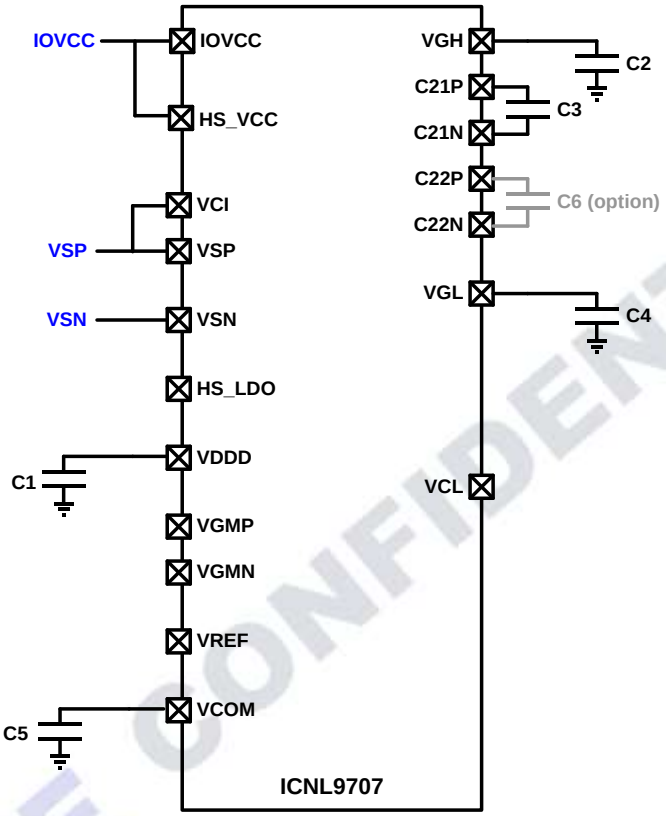
8.3.32 DGC_B_L

Inst / Para		D7	D6	D5	D4	D3	D2	D1	D0	HEX
DGC_B_L		1	1	1	0	1	1	0	1	EDh
Parameter	1	DGC_B_V255[1:0]		DGC_B_V254[1:0]		DGC_B_V252[1:0]		DGC_B_V250[1:0]		00h
	2	DGC_B_V248[1:0]		DGC_B_V244[1:0]		DGC_B_V240[1:0]		DGC_B_V232[1:0]		00h
	3	DGC_B_V224[1:0]		DGC_B_V208[1:0]		DGC_B_V192[1:0]		DGC_B_V160[1:0]		00h
	4	DGC_B_V128[1:0]		DGC_B_V127[1:0]		DGC_B_V95[1:0]		DGC_B_V63[1:0]		00h
	5	DGC_B_V47[1:0]		DGC_B_V31[1:0]		DGC_B_V23[1:0]		DGC_B_V15[1:0]		00h
	6	DGC_B_V11[1:0]		DGC_B_V7[1:0]		DGC_B_V5[1:0]		DGC_B_V3[1:0]		00h
	7	DGC_B_V1[1:0]		DGC_B_V0[1:0]		0	0	0	0	00h

Description	
DGC_B_V255[1:0]	Set Level_255 of Blue data.
DGC_B_V254[1:0]	Set Level_254 of Blue data.
DGC_B_V252[1:0]	Set Level_252 of Blue data.
DGC_B_V250[1:0]	Set Level_250 of Blue data.
DGC_B_V248[1:0]	Set Level_248 of Blue data.
DGC_B_V244[1:0]	Set Level_244 of Blue data.
DGC_B_V240[1:0]	Set Level_240 of Blue data.
DGC_B_V232[1:0]	Set Level_232 of Blue data.
DGC_B_V224[1:0]	Set Level_224 of Blue data.
DGC_B_V208[1:0]	Set Level_208 of Blue data.
DGC_B_V192[1:0]	Set Level_192 of Blue data.
DGC_B_V160[1:0]	Set Level_160 of Blue data.
DGC_B_V128[1:0]	Set Level_128 of Blue data.
DGC_B_V127[1:0]	Set Level_127 of Blue data.
DGC_B_V95[1:0]	Set Level_95 of Blue data.
DGC_B_V63[1:0]	Set Level_63 of Blue data.
DGC_B_V47[1:0]	Set Level_47 of Blue data.
DGC_B_V31[1:0]	Set Level_31 of Blue data.
DGC_B_V23[1:0]	Set Level_23 of Blue data.
DGC_B_V15[1:0]	Set Level_15 of Blue data.
DGC_B_V11[1:0]	Set Level_11 of Blue data.
DGC_B_V7[1:0]	Set Level_7 of Blue data.
DGC_B_V5[1:0]	Set Level_5 of Blue data.
DGC_B_V3[1:0]	Set Level_3 of Blue data.
DGC_B_V1[1:0]	Set Level_1 of Blue data.
DGC_B_V0[1:0]	Set Level_0 of Blue data.

9. Application

9.1 Reference components for 3_Power_mode application

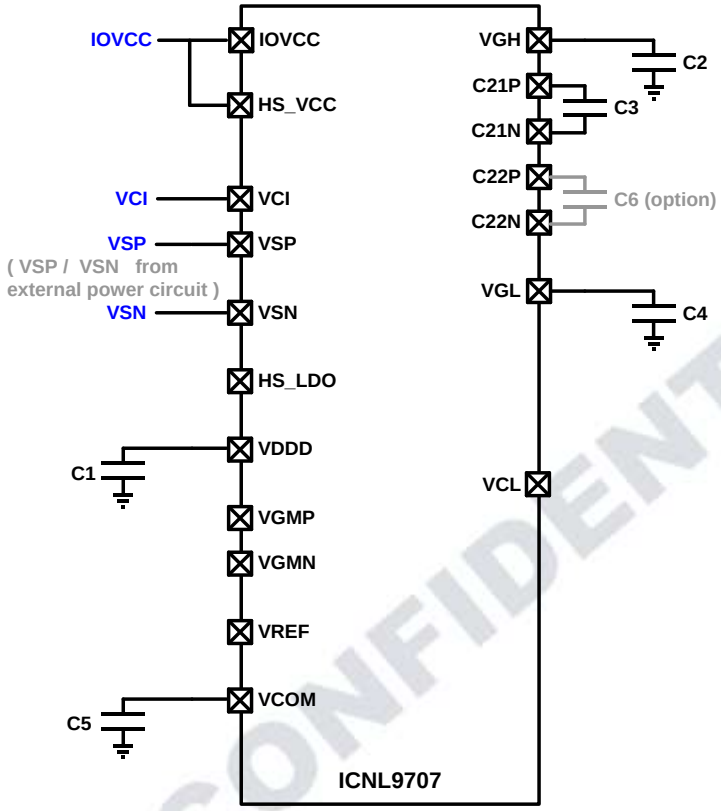


Pad Name	Symbol	Connection	Recommended spec	Remark
VDDD	C1	VDDD ⊕—| |—⊖ GND	1 uF, Max. 6V	
VGH	C2	VGH ⊕—| |—⊖ GND	1 uF, Max. 25V	
C21P-C21N	C3	C21P ⊕—| |—⊖ C21N	1 uF, Max. 25V	
VGL	C4	VGL ⊕—| |—⊖ GND	1 uF, Max. 25V	
VCOM	C5	VCOM ⊕—| |—⊖ GND	1 uF, Max. 6V	
C22P-C22N	C6	C22P ⊕—| |—⊖ C22N	1 uF, Max. 25V	Optional

Note 1. Required components: 5C / 0D.

Note 2. C6 is optional for panels spec using VGH/VGL> +/- 15V.

9.2 Reference components for 2_Power_mode application



Pad Name	Symbol	Connection	Recommended spec	Remark
VDDD	C1	VDDD ⊕—| |—⊖ GND	1 uF, Max. 6V	
VGH	C2	VGH ⊕—| |—⊖ GND	1 uF, Max. 25V	
C21P-C21N	C3	C21P ⊕—| |—⊖ C21N	1 uF, Max. 25V	
VGL	C4	VGL ⊕—| |—⊖ GND	1 uF, Max. 25V	
VCOM	C5	VCOM ⊕—| |—⊖ GND	1 uF, Max. 6V	
C22P-C22N	C6	C22P ⊕—| |—⊖ C22N	1 uF, Max. 25V	Optional (*2)

Note 1. Required components: 5C / 0D, exclude from external power components.

Note 2. C6 is optional for panels spec using VGH/VGL> +/- 15V.

9.3 Maximum Layout Resistance

Recommended maximum Panel ITO layout series resistance:

No.	Name	Max. series R	No.	Name	Max. series R
1 - 2	DUMMY	NA	263 - 264	PCLK	100
3	CGOUT_L1	10	265 - 266	DCX	100
4	CGOUT_L2	10	267 - 268	CSX	100
5	CGOUT_L3	10	269 - 270	SCL	100
6	CGOUT_L4	10	271 - 272	SDI	100
7	CGOUT_L5	10	273 - 274	SDO	100
8	CGOUT_L6	10	275 - 278	CABC_PWM_OUT	100
9	CGOUT_L7	10	279 - 284	TE	100
10	CGOUT_L8	10	285 - 290	TE_TOUCH	100
11	CGOUT_L9	10	291 - 294	RESX	100
12	CGOUT_L10	10	295 - 296	TEST0	100
13	CGOUT_L11	10	297 - 298	TEST1	100
14	CGOUT_L12	10	299 - 300	TEST2	100
15	CGOUT_L13	10	301 - 302	VSSD	5
16	CGOUT_L14	10	303 - 304	BS0	100
17	CGOUT_L15	10	305 - 306	IOVCC	5
18	CGOUT_L16	10	307 - 308	BS1	100
19	CGOUT_L17	10	309 - 310	VSSD	5
20	CGOUT_L18	10	311 - 312	DUMMY	NA
21	CGOUT_L19	10	313 - 314	IOVCC	5
22	CGOUT_L20	10	315 - 316	DUMMY	NA
23	CGOUT_L21	10	317 - 318	VSSD	5
24	CGOUT_L22	10	319 - 320	BS2	100
25 - 27	VCOM	10	321 - 322	IOVCC	5
28 - 37	VSSA	5	323 - 324	PCCS0	100
38 - 39	VTESTOUTN	100	325 - 326	VSSD	5
40	HS_VSS	5	327 - 328	PCCS1	100
41 - 46	HS_D0N	5	329 - 338	IOVCC	5
47 - 52	HS_D0P	5	339 - 348	VDDD	5
53	HS_VSS	5	349 - 358	VSSD	5
54 - 59	HS_D1N	5	359 - 366	VCSW2	20
60 - 65	HS_D1P	5	367 - 374	VCSW1	20
66	HS_VSS	5	375 - 380	VPP	10
67 - 72	HS_CKN	5	381 - 382	VTESTOUTP	100
73 - 78	HS_CKP	5	383 - 387	VCI	5
79	HS_VSS	5	388 - 395	VSSD	5

No.	Name	Max. series R	No.	Name	Max. series R
80 - 85	HS_D2N	5	396 - 399	VSSAC	5
86 - 91	HS_D2P	5	400 - 406	VSSA	5
92	HS_VSS	5	407 - 409	VGMP	5
93 - 98	HS_D3N	5	410 - 412	VGMN	5
99 - 104	HS_D3P	5	413 - 415	VREF	20
105 - 116	HS_VSS	5	416 - 420	VSSD	5
117 - 128	HS_LDO	5	421 - 428	VCI	5
129 - 140	HS_VCC	5	429 - 433	VCL	5
141 - 155	IOVCC	5	434 - 440	DUMMY	NA
156 - 170	VDDD	5	441 - 447	DUMMY	NA
171 - 185	VSSD	5	448 - 454	DUMMY	NA
186	TS7	100	455 - 461	DUMMY	NA
187	TS6	100	462 - 468	VSP	5
188	TS5	100	469 - 475	VSN	5
189	TS4	100	476 - 482	C21P	5
190	TS3	100	483 - 489	C21N	5
191	TS2	100	490 - 496	C22P	5
192	TS1	100	497 - 503	C22N	5
193	TS0	100	504 - 509	VGH	5
194 - 199	VSP	5	510 - 515	VCI	5
200 - 201	DUMMY	NA	516 - 519	VSSA	5
202 - 203	TEST_OSC	100	520 - 523	VSSD	5
204 - 208	VSSD	5	524 - 530	DUMMY	NA
209	DUMMY	NA	531 - 537	DUMMY	NA
210	DUMMY	NA	538 - 544	DUMMY	NA
211	DUMMY	NA	545 - 551	DUMMY	NA
212	DUMMY	NA	552 - 557	VGL	5
213	DUMMY	NA	558 - 564	VCI	5
214	DUMMY	NA	565 - 571	VSSD	5
215	DUMMY	NA	572 - 577	VGL	5
216	DUMMY	NA	578 - 581	DUMMY	NA
217	DUMMY	NA	582 - 584	VCOM	5
218	DUMMY	NA	585	CGOUT_R22	10
219	DUMMY	NA	586	CGOUT_R21	10
220	DUMMY	NA	587	CGOUT_R20	10
221	DUMMY	NA	588	CGOUT_R19	10
222	DUMMY	NA	589	CGOUT_R18	10
223	DUMMY	NA	590	CGOUT_R17	10
224	DUMMY	NA	591	CGOUT_R16	10

No.	Name	Max. series R	No.	Name	Max. series R
225	DB_7	100	592	CGOUT_R15	10
226	DB_6	100	593	CGOUT_R14	10
227	DB_5	100	594	CGOUT_R13	10
228	DB_4	100	595	CGOUT_R12	10
229	DB_3	100	596	CGOUT_R11	10
230	DB_2	100	597	CGOUT_R10	10
231	DB_1	100	598	CGOUT_R9	10
232	DB_0	100	599	CGOUT_R8	10
233 - 234	DUMMY	NA	600	CGOUT_R7	10
235 - 238	VSN	5	601	CGOUT_R6	10
239 - 240	BIST	100	602	CGOUT_R5	10
241 - 248	DUMMY	NA	603	CGOUT_R4	10
249 - 256	DUMMY	NA	604	CGOUT_R3	10
257 - 258	HSYNC	100	605	CGOUT_R2	10
259 - 260	VSYNC	100	606	CGOUT_R1	10
261 - 262	DE	100	607 - 608	DUMMY	NA

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11. Revision History

Version	Revisions	Date	Modified by
V0.01	First edition	July 2018	ZY